DCDC BOOST EMI

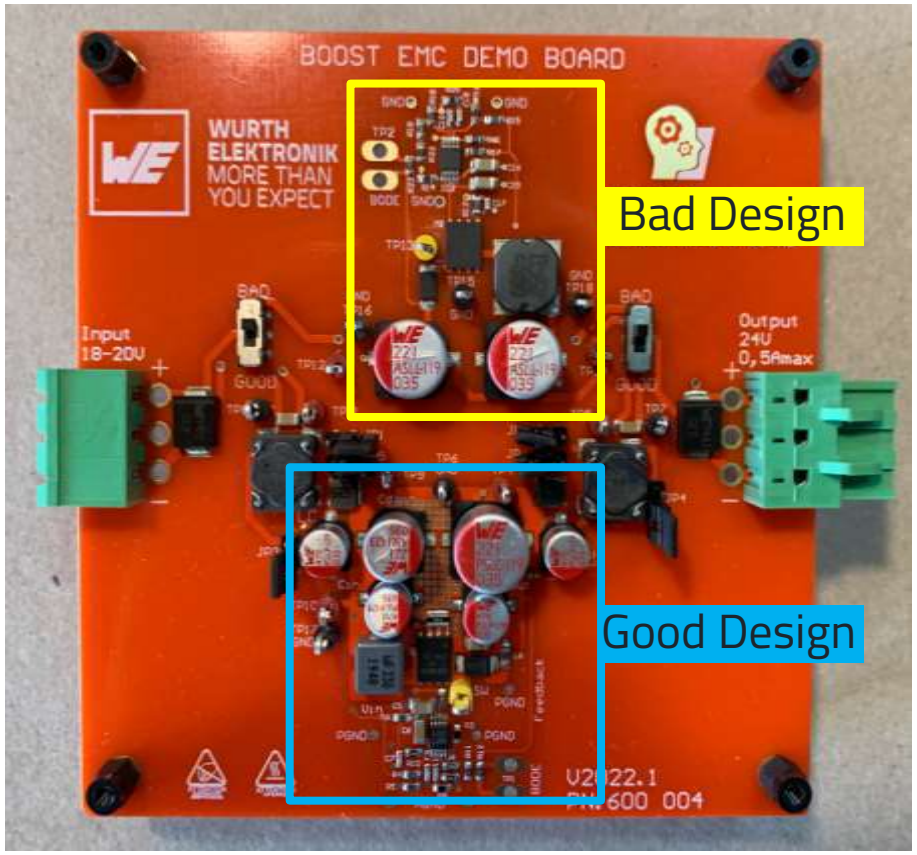
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

- Overview and Key Points
- Schematic in Detail
- PCB in Detail
- Calculations
- Time Domain Measurements
- Redexpert & LT Spice Simulations
- EMC Measurements from the Lab
- EMC Measurements from the workbench

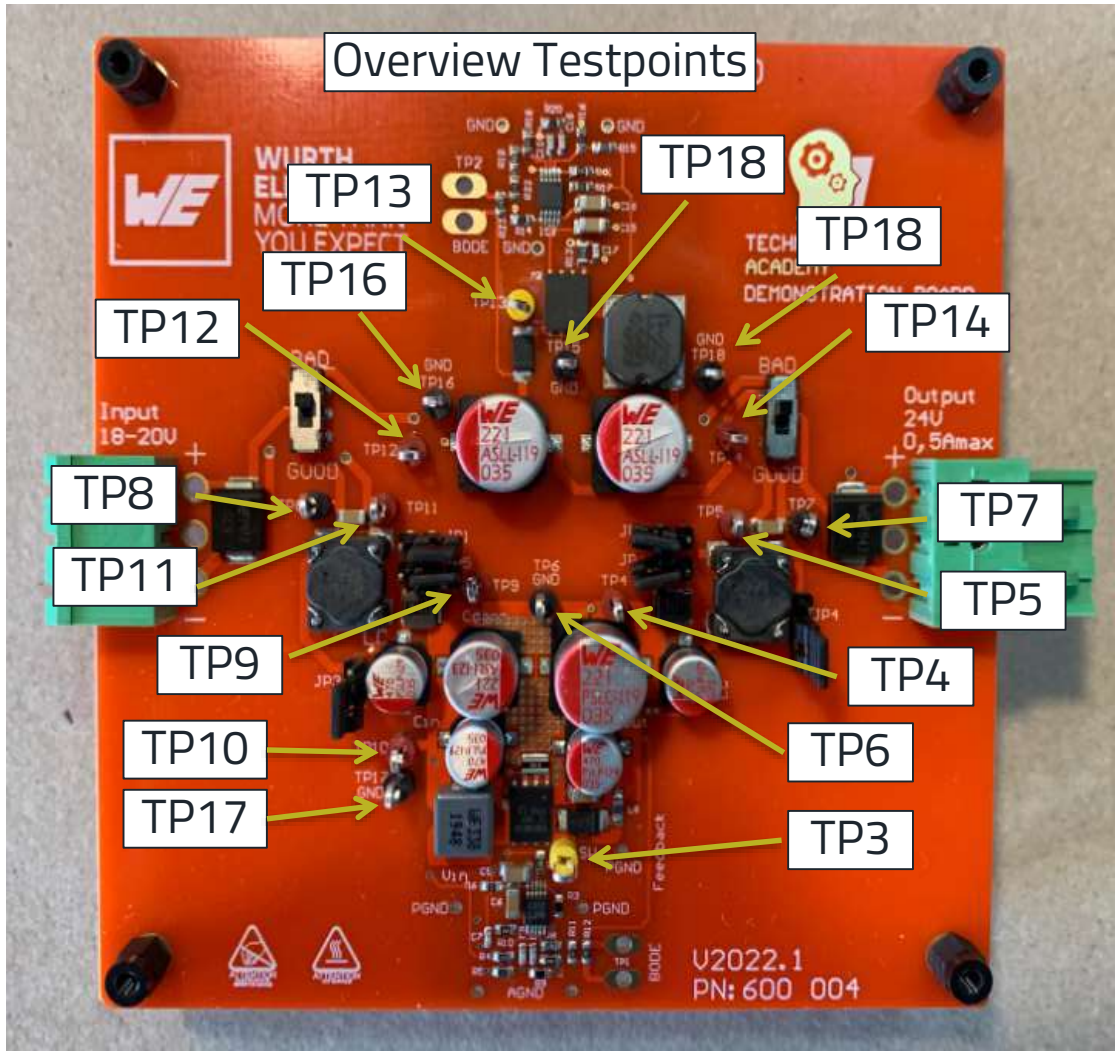
Objective of the Good and Bad Layout

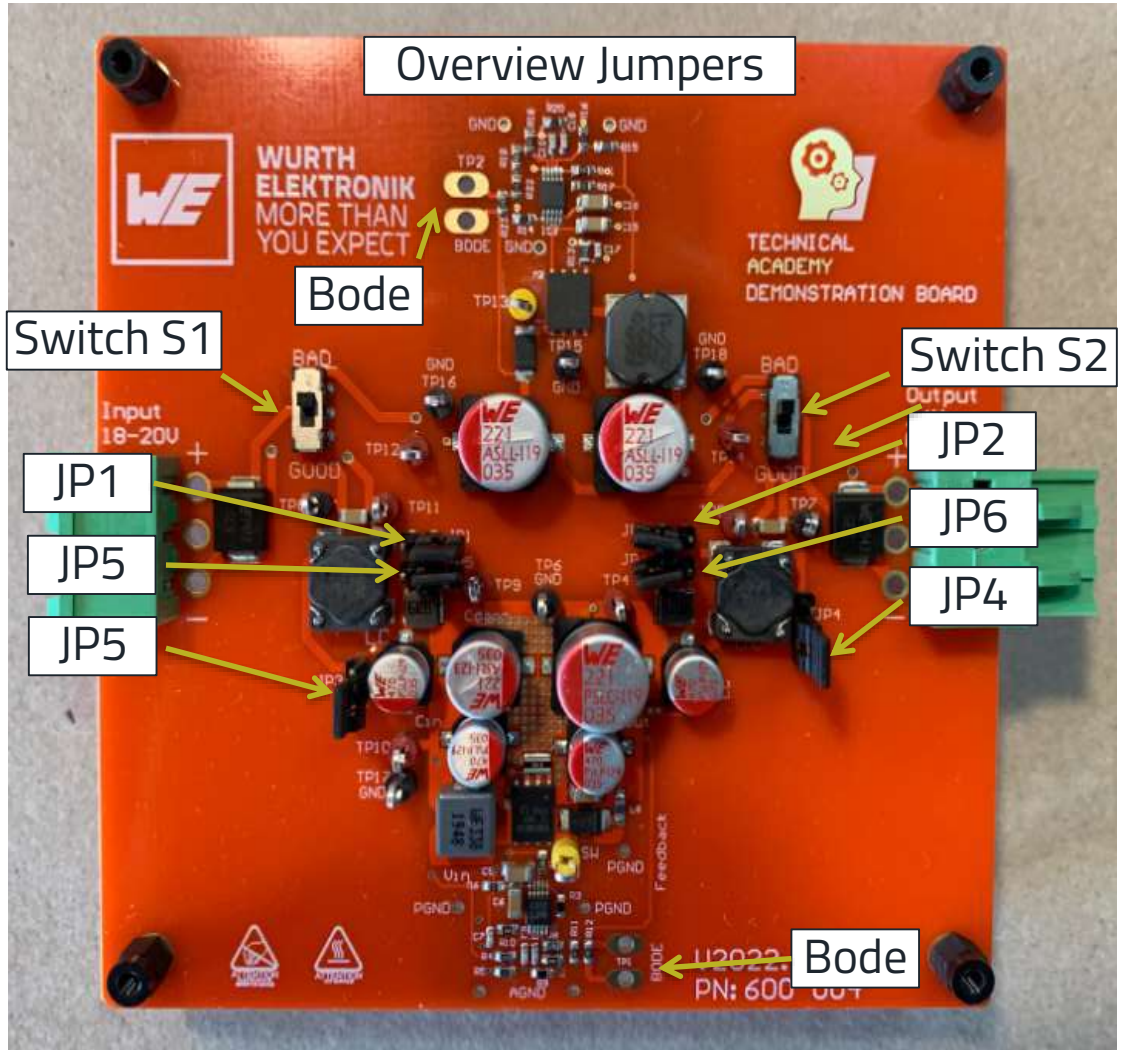
Keypoints

- Single Point PGND vs. big PGND Loop
- Correct vs. Wrong Capacitor Position
- Same Semiconductors, different Passives
- Shielded Choke vs. Unshielded Choke
- Alu-Electrolyte vs. Polymer Caps
- Filter @ I/Os vs. No Filter at all
- Ferrite in the Power Loop of a DCDC



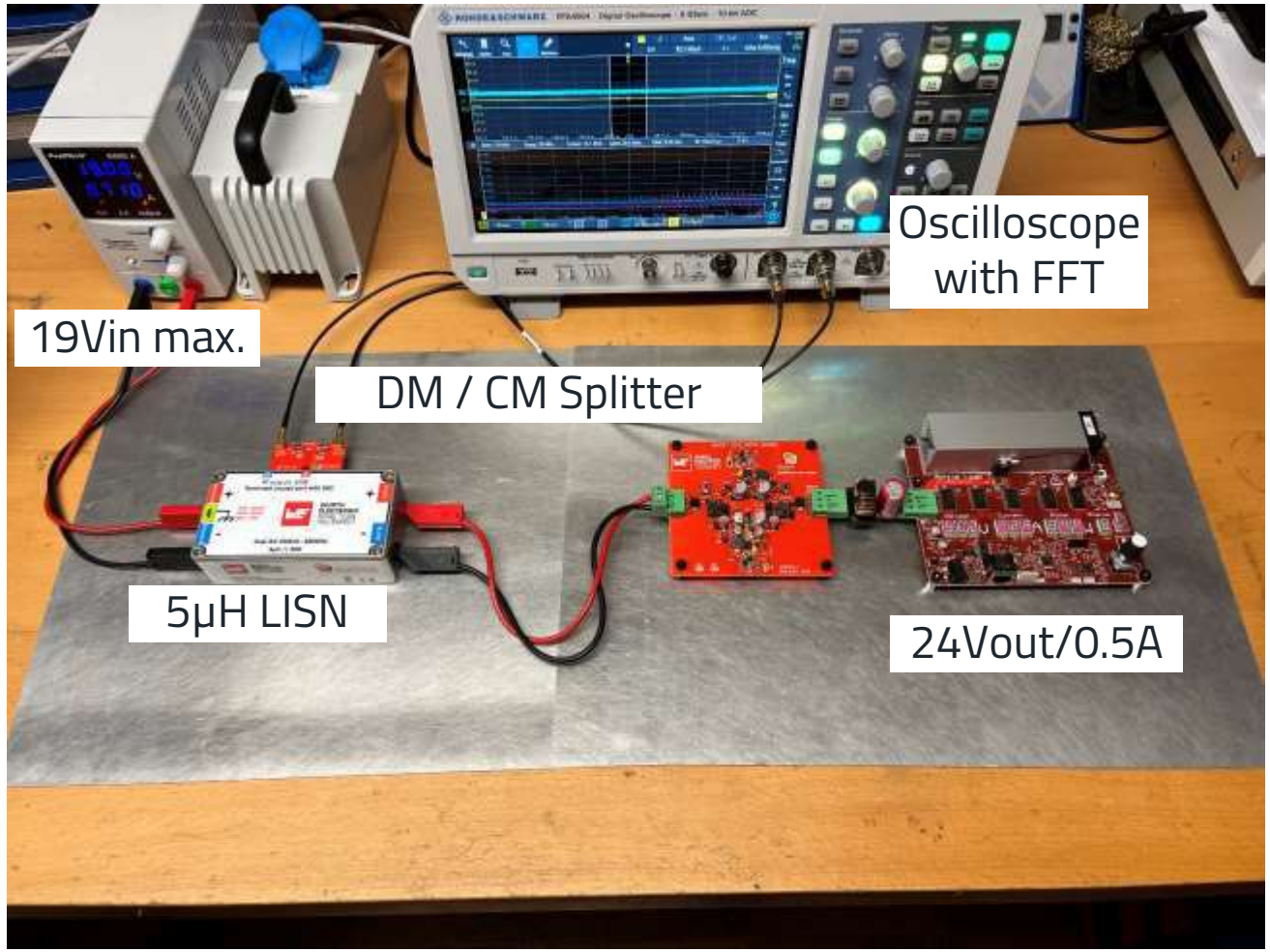
PCB Overview





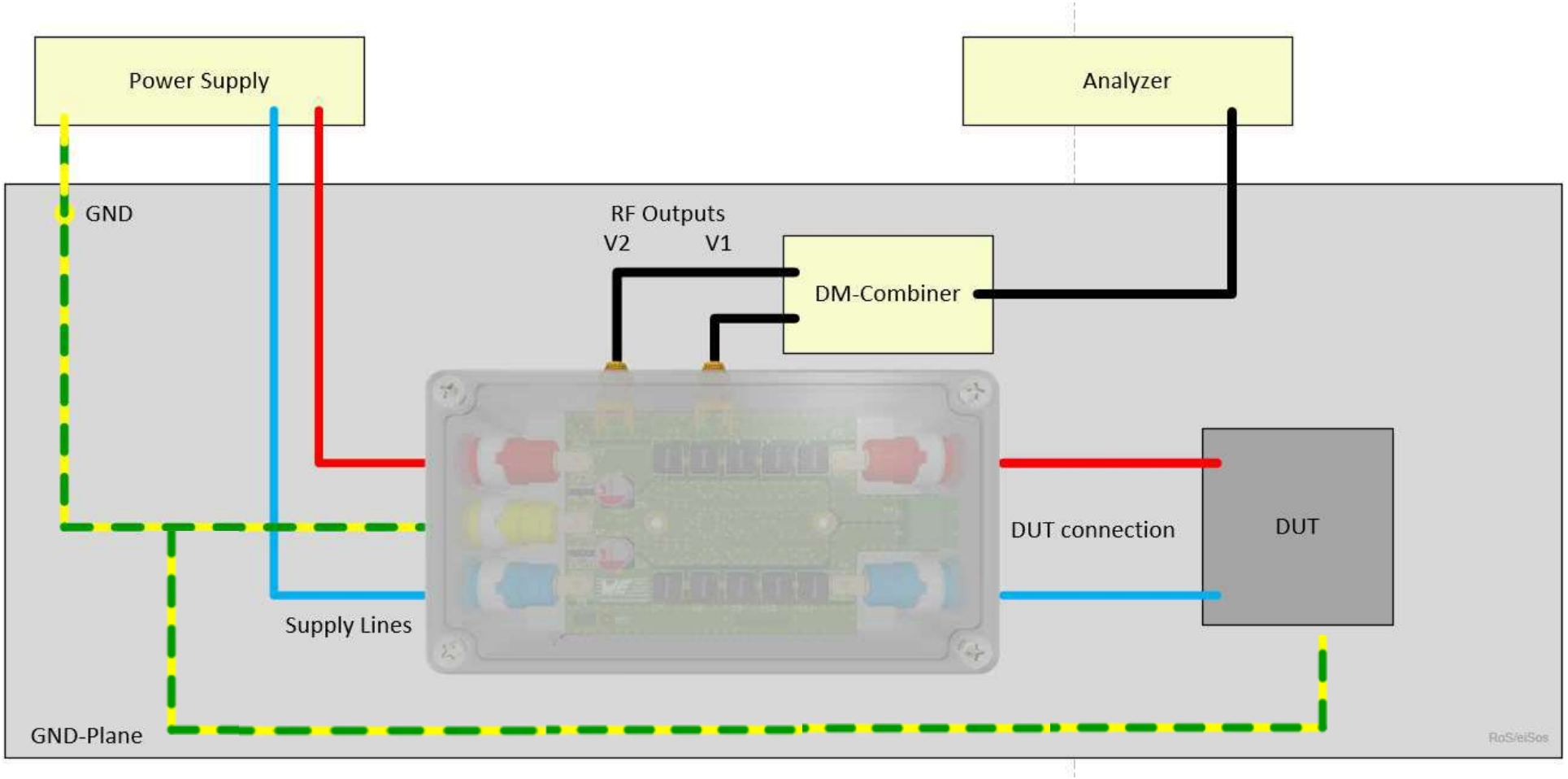
Setup

Use the new FAE or Ohmic load (48ohm@12Wmax.)



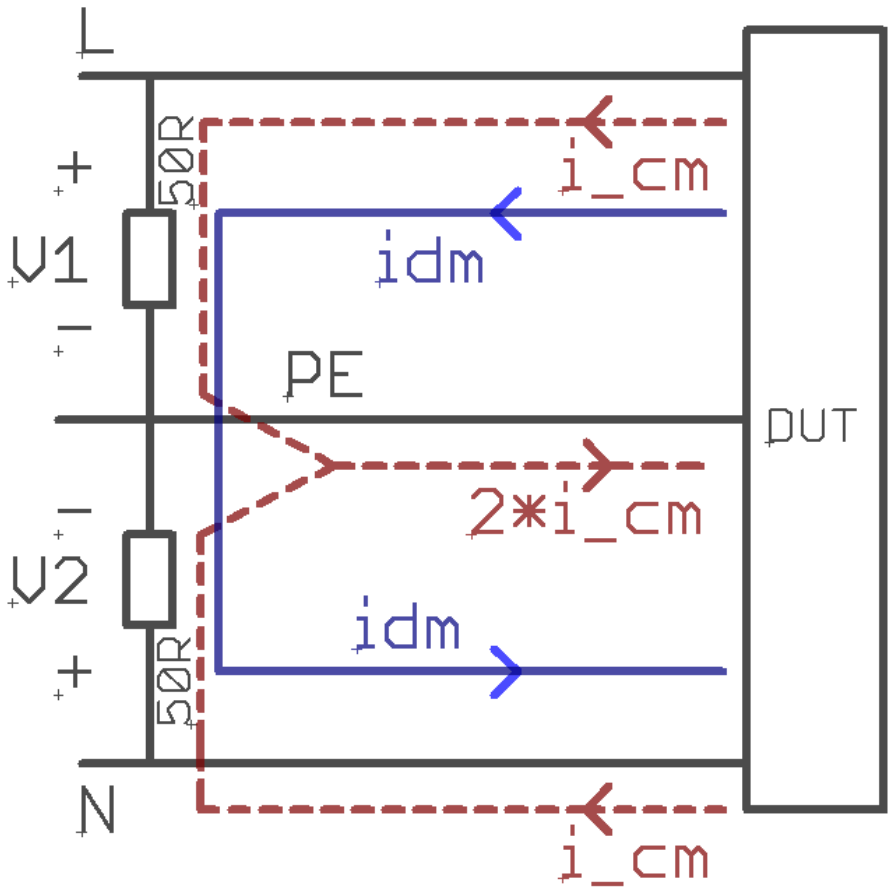
Splitter/Combiner for DM/CM

Setup: RTA4004 / 5µH LISN / CM&DM Splitter



Measure CM and DM separatly

Currents through LISN



$$V_1 = 50\Omega(i_{dm} + i_{cm})$$

$$V_2 = 50\Omega(-i_{dm} + i_{cm})$$

- Differential Mode

  $$V_{dm} = 50\Omega i_{dm} = 0,5(V_1 - V_2)$$

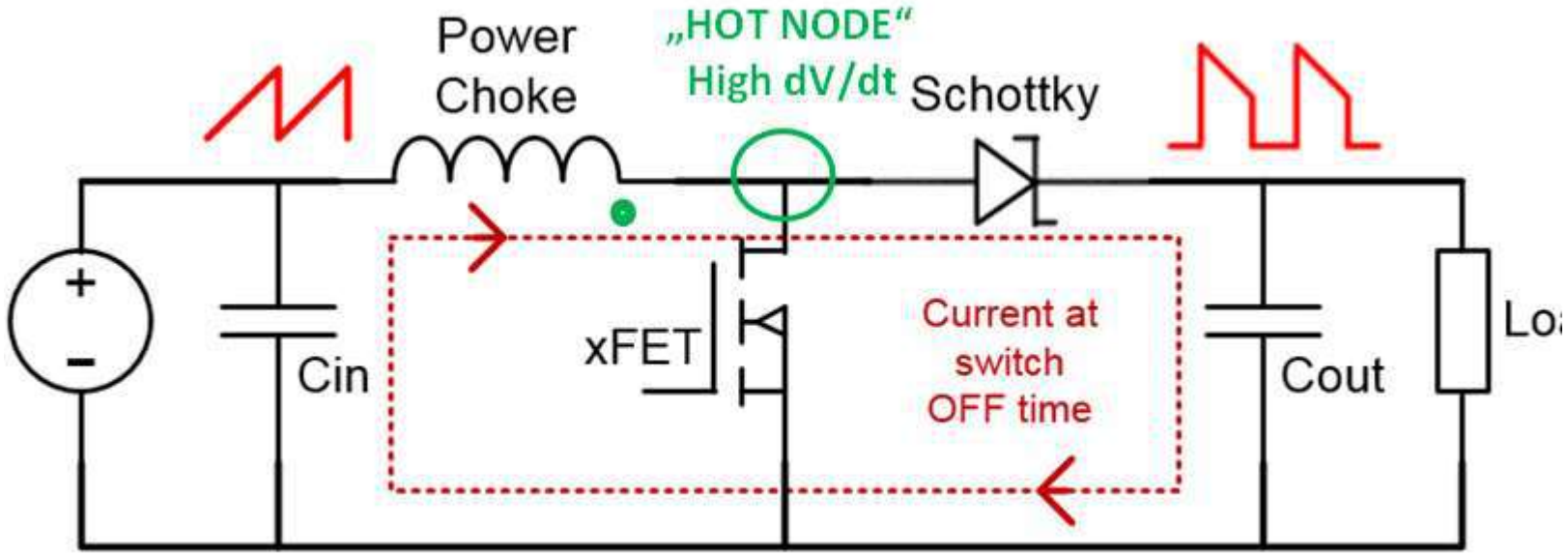
- Common Mode

  $$V_{cm} = 50\Omega i_{cm} = 0,5(V_1 + V_2)$$

Example BOOST DCDC

EMI Overview

Source of Differential Mode Source of Common Mode

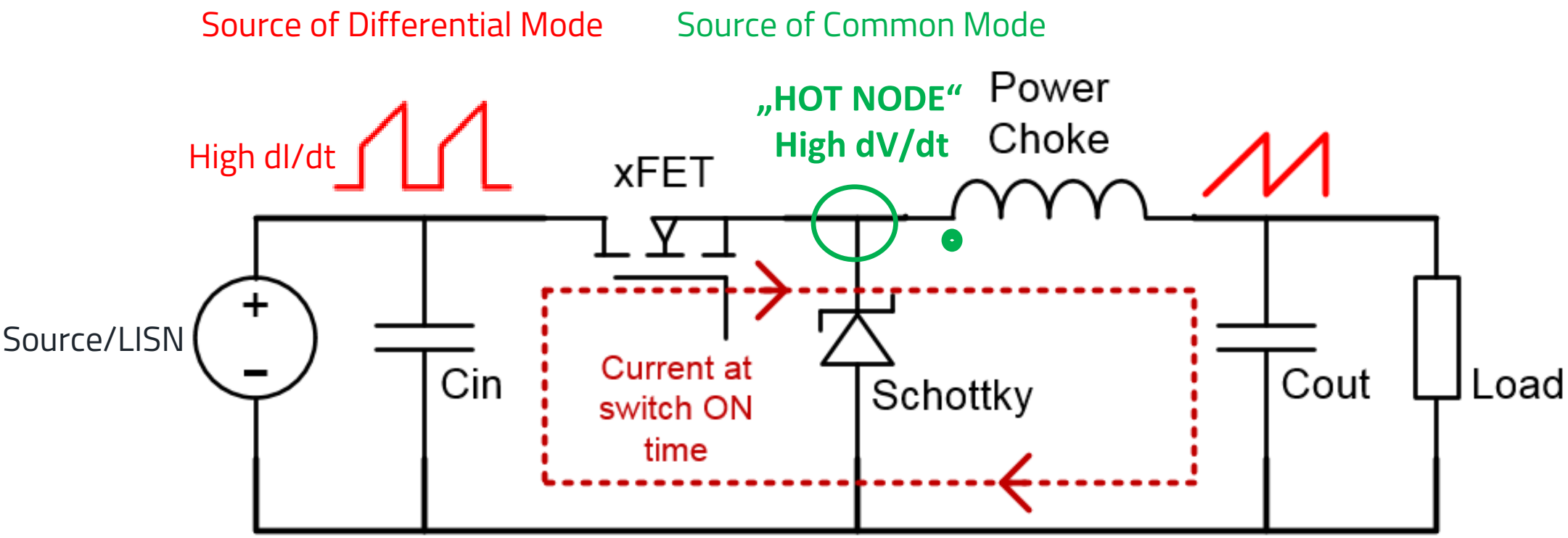


$$U_{DM} = L_{parasitic} \cdot \frac{dI}{dt}$$

$$I_{CM} = C_{parasitic} \cdot \frac{dV}{dt}$$

Example Buck DCDC

EMI Overview

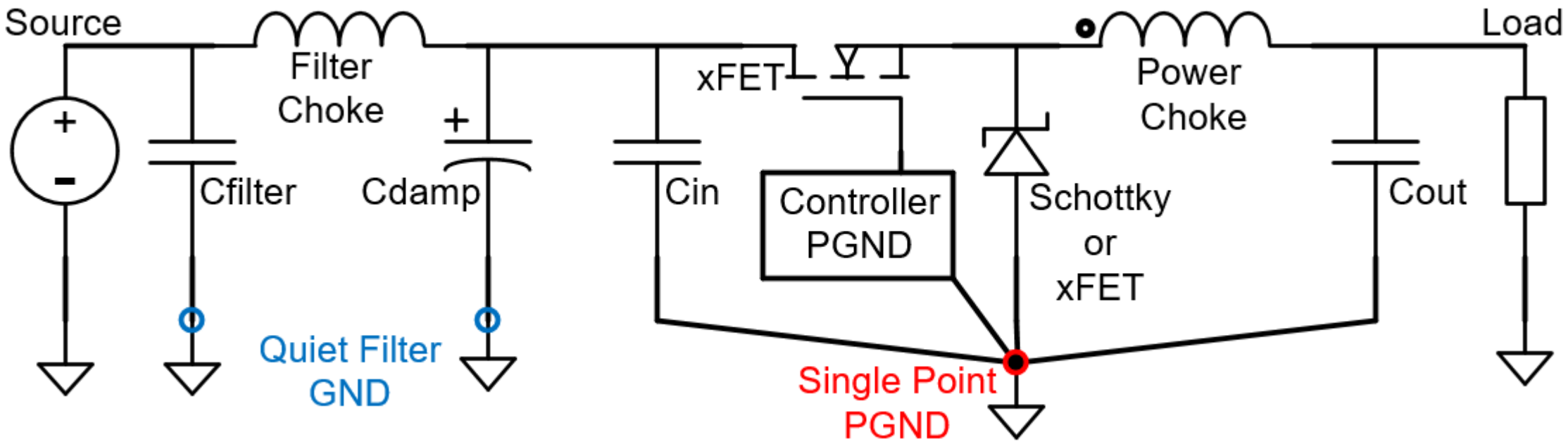


$$U_{DM} = L_{parasitic} \cdot \frac{dI}{dt}$$

$$I_{CM} = C_{parasitic} \cdot \frac{dV}{dt}$$

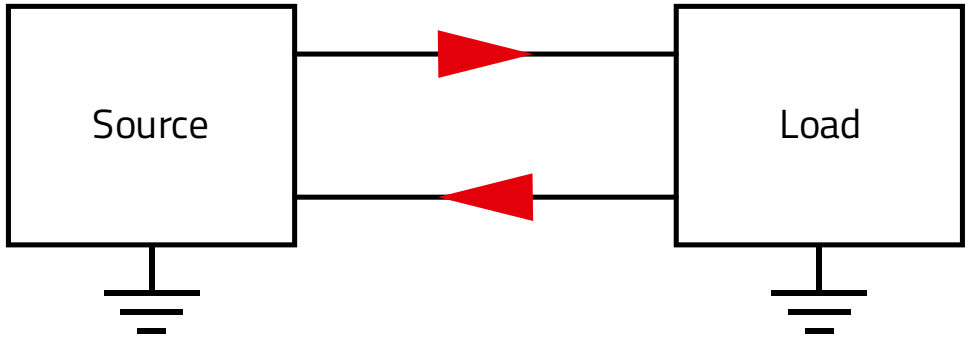
Single Point Power GND for Buck / Boost / SEPIC etc.

Layout Key Points



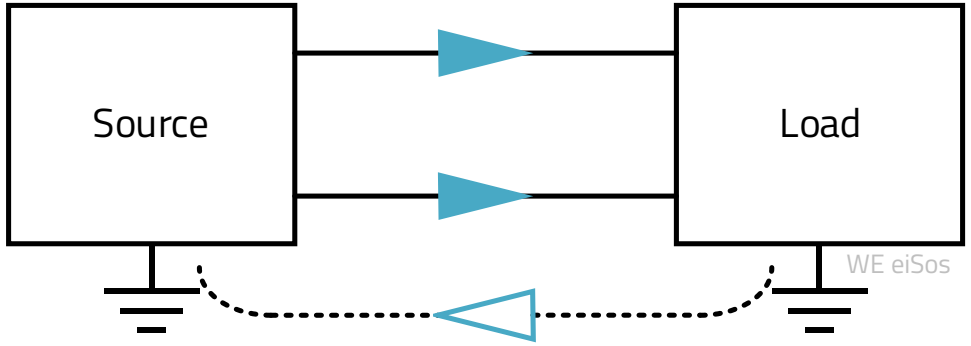
Noise Transmission Modes

Differential Mode



- Noise and useful signal use the same paths
- Earth is not affected

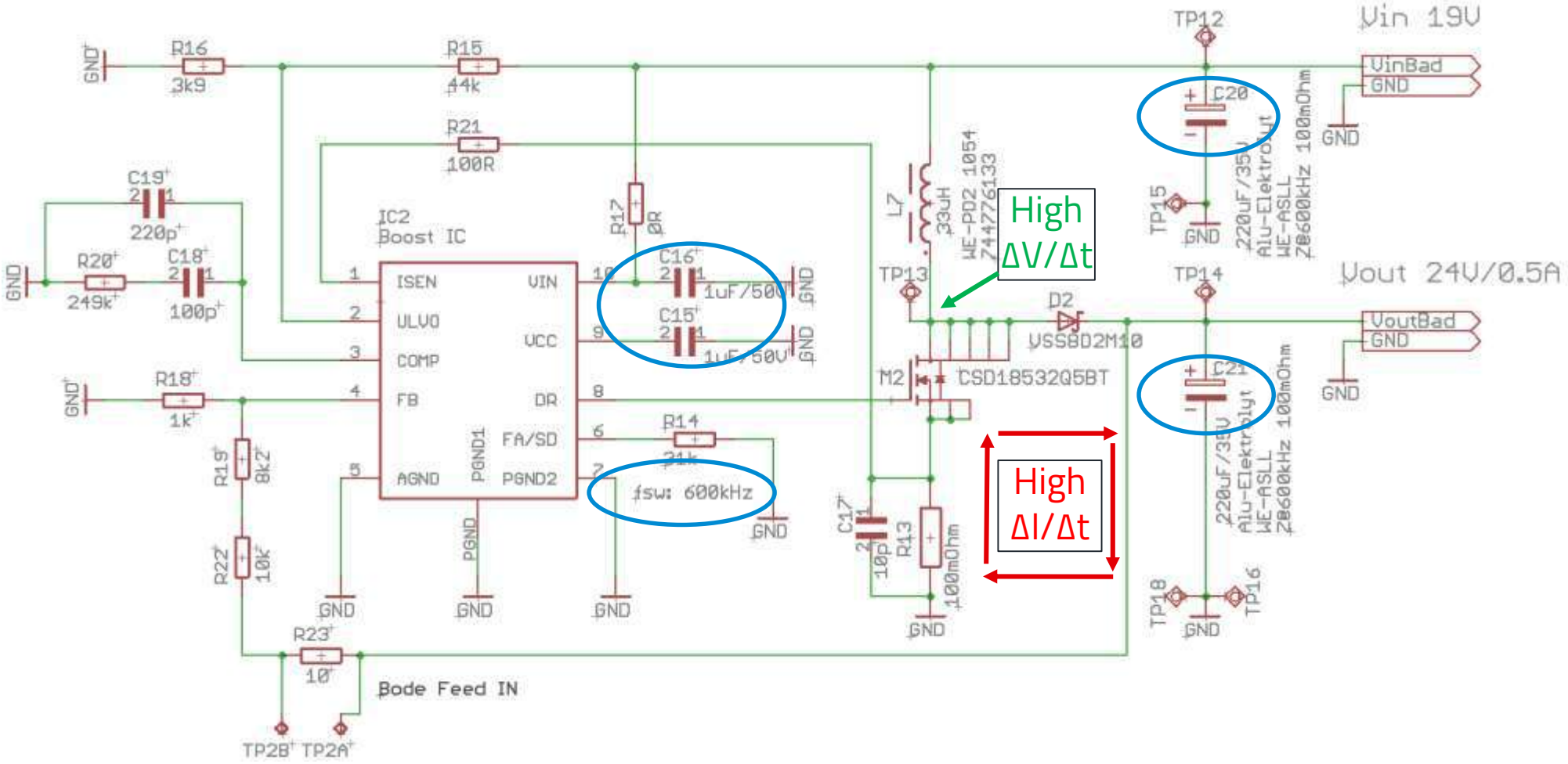
Common Mode



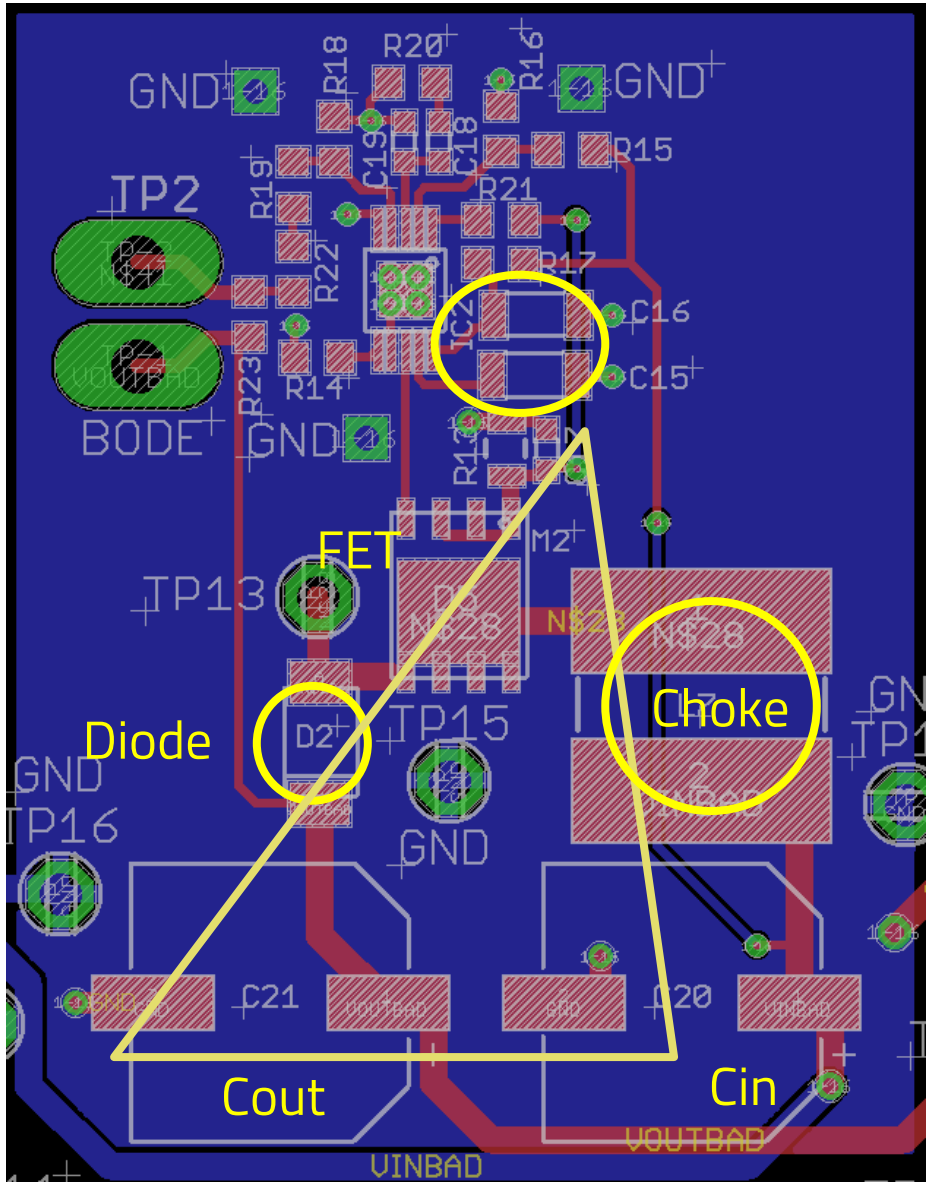
- Noise uses both lines in same direction
- Earth is used a return path

Schematic Bad Design

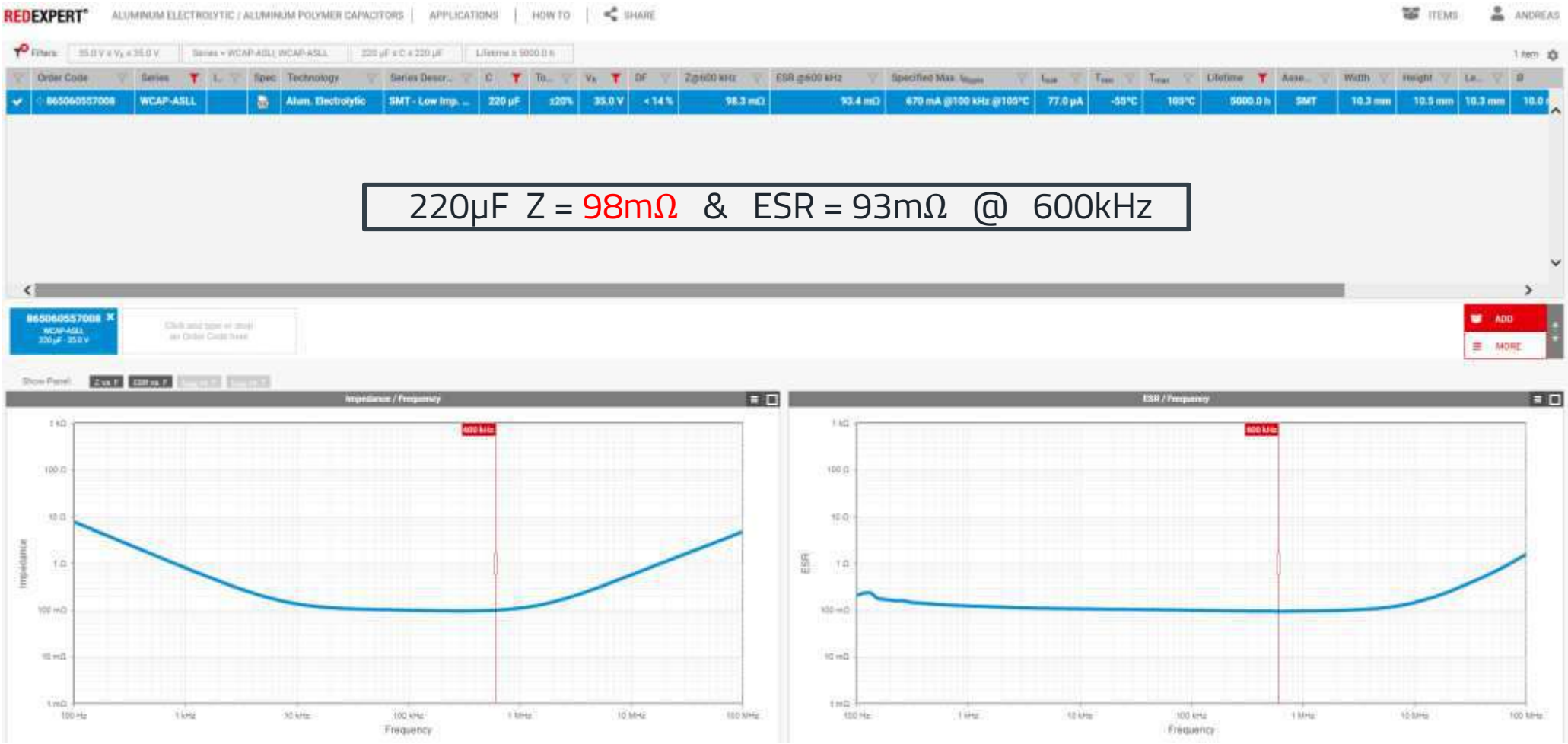
19V → 24V/0,5A



PCB Layout Bad Design



Redexpert Alu-Elko Cap Selection for Fsw 600kHz



Conducted EMI Calculation with 220µF Elko Cin

Triangular approximation(differntail mode only):

$$D = \frac{U_{out} - U_{in} + U_d}{U_{out} + U_d} = \frac{24V - 19V + 0{,}5V}{24V + 0{,}5V} = 0{,}224$$

$$\Delta I = \frac{U_{in}}{L \cdot f_{sw}} \cdot D = \frac{19V}{33\mu H \cdot 600kHz} \cdot 0{,}224 = 0{,}21A$$

$$|I_{cin}[600kHz]| = \frac{\Delta I}{\sqrt{2} \cdot \pi^2 \cdot D \cdot (1 - D)} \cdot |\sin(\pi \cdot D)| = \frac{0{,}21A}{\sqrt{2} \cdot \pi^2 \cdot 0{,}224 \cdot (1 - 0{,}224)} \cdot |\sin(\pi \cdot 0{,}224)| = 56mA$$

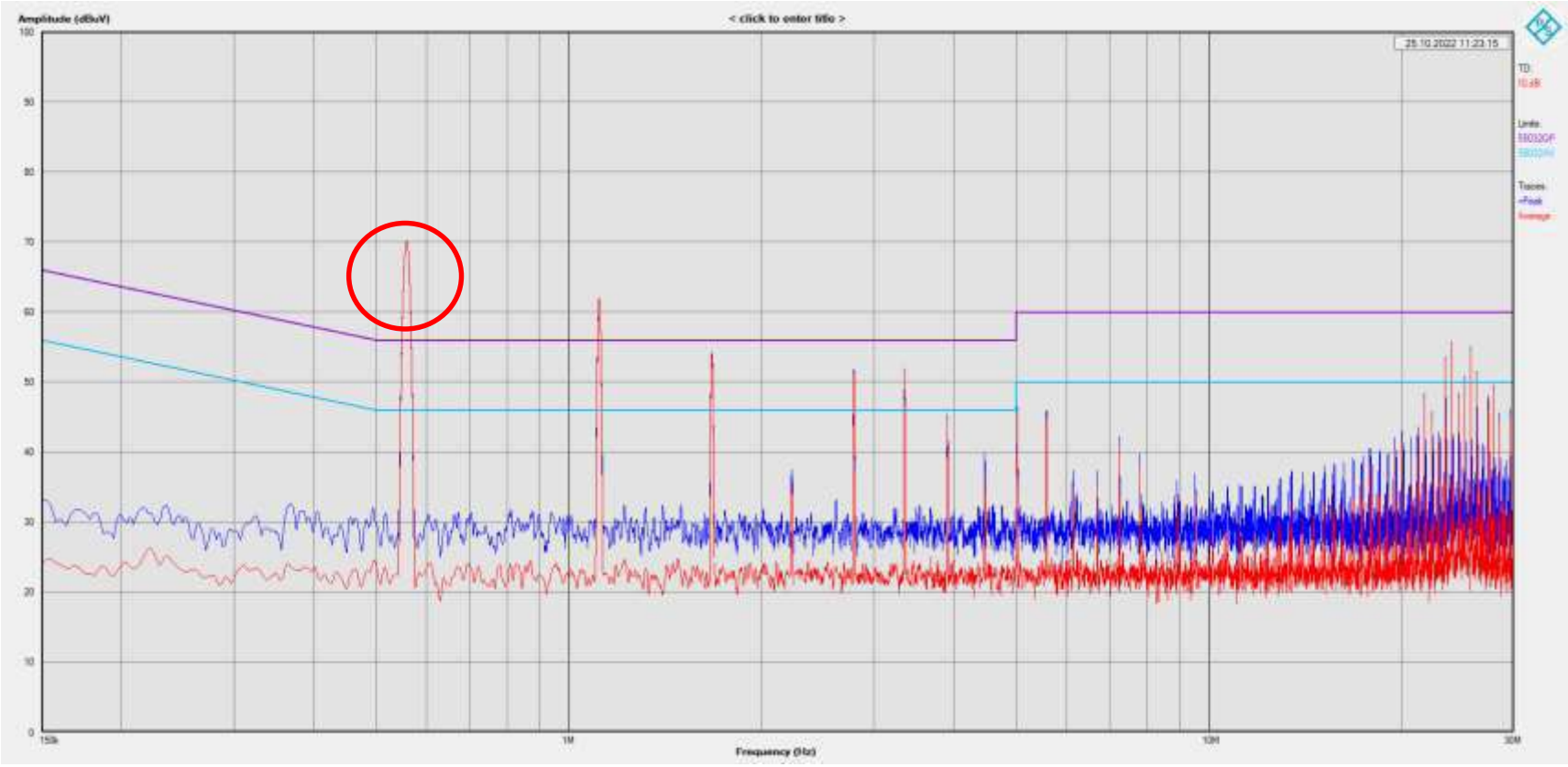
$$|U_{cin}(600kHz)| = |Z_{cin}(600kHz)| \cdot |I_{cin}(600kHz)| = 98m\Omega \cdot 56mA = 5{,}49mV$$

$$5{,}49mV \rightarrow 20\log\left(\frac{5{,}49mV}{1\mu V}\right) = 74{,}8dB\mu V \ - 6dB\mu V(LISN\ Voltage\ Divider) = 68{,}8dB\mu V$$

Limit CISPR32 Class B is 46dBµV → approx. 30dB Damping is necessary

Verification of the triangular approximation BAD Design

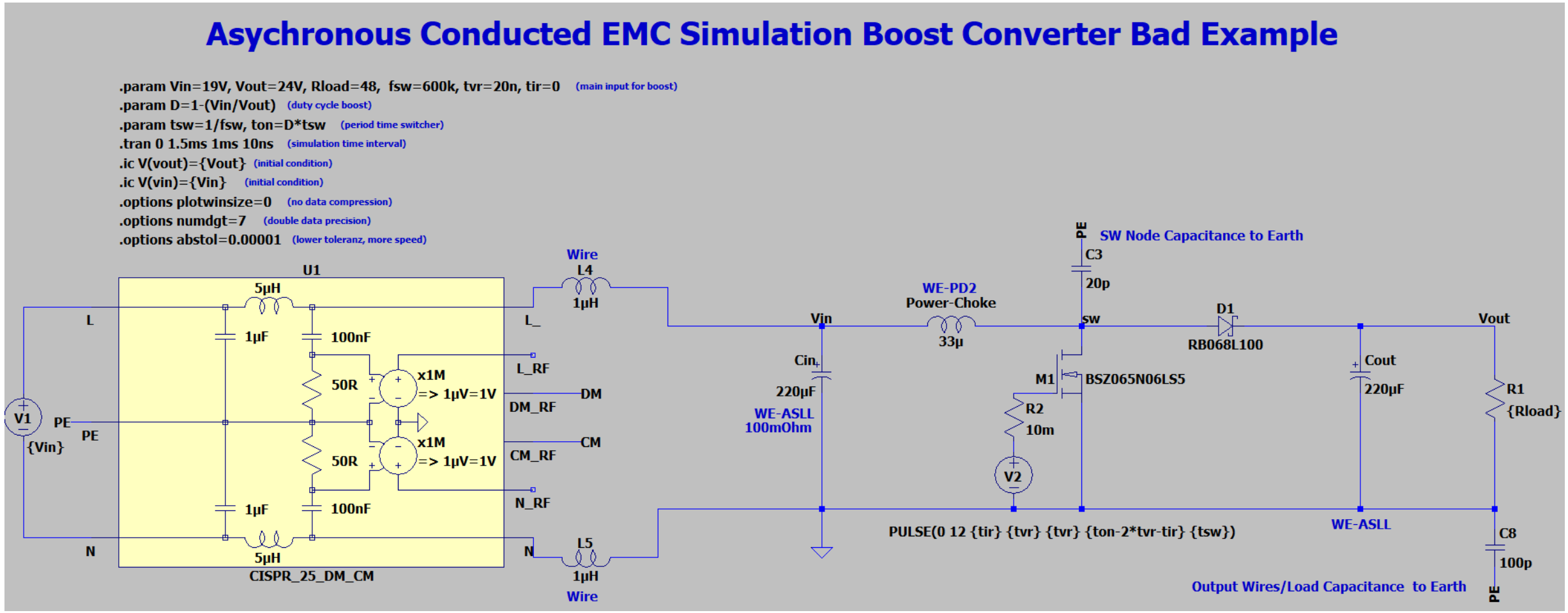
Measure DM noise on input with DM/CM splitter



69dBµV as calculated

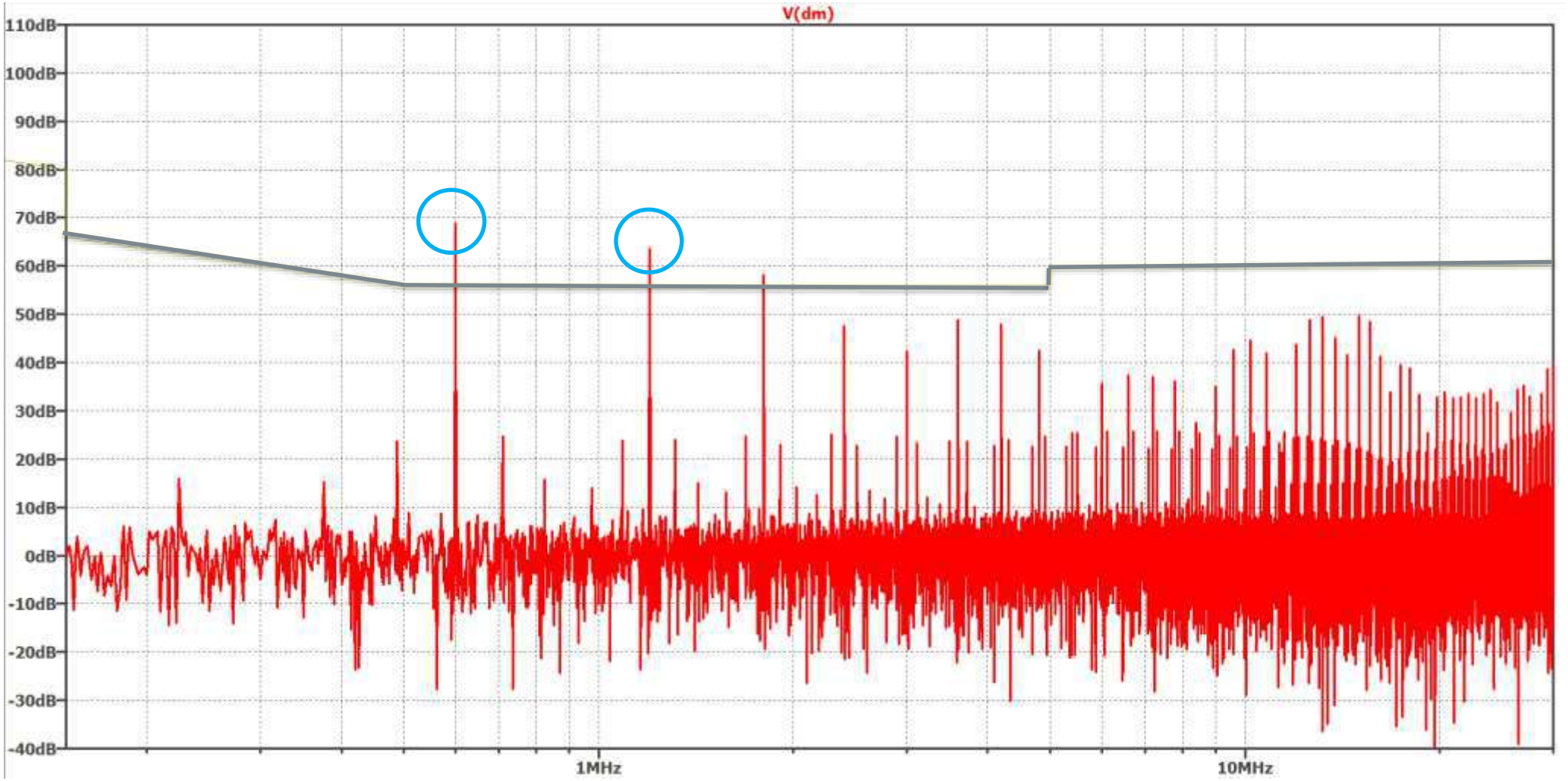
LT Spice Boost BAD Simulation

Simple Model to double check the calculation



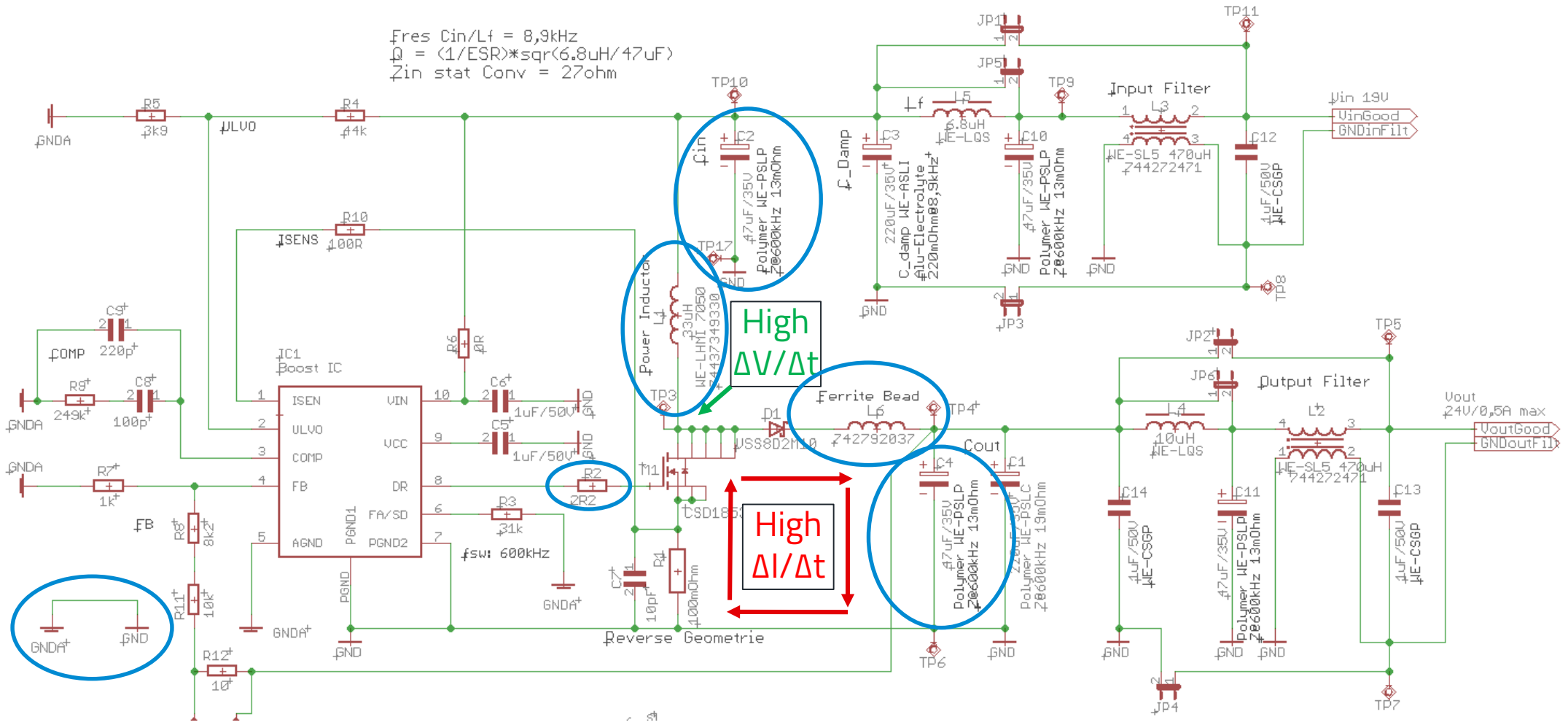
Simulated DM Noise with LT Spice

FFT Plot of the LISN DM Channel

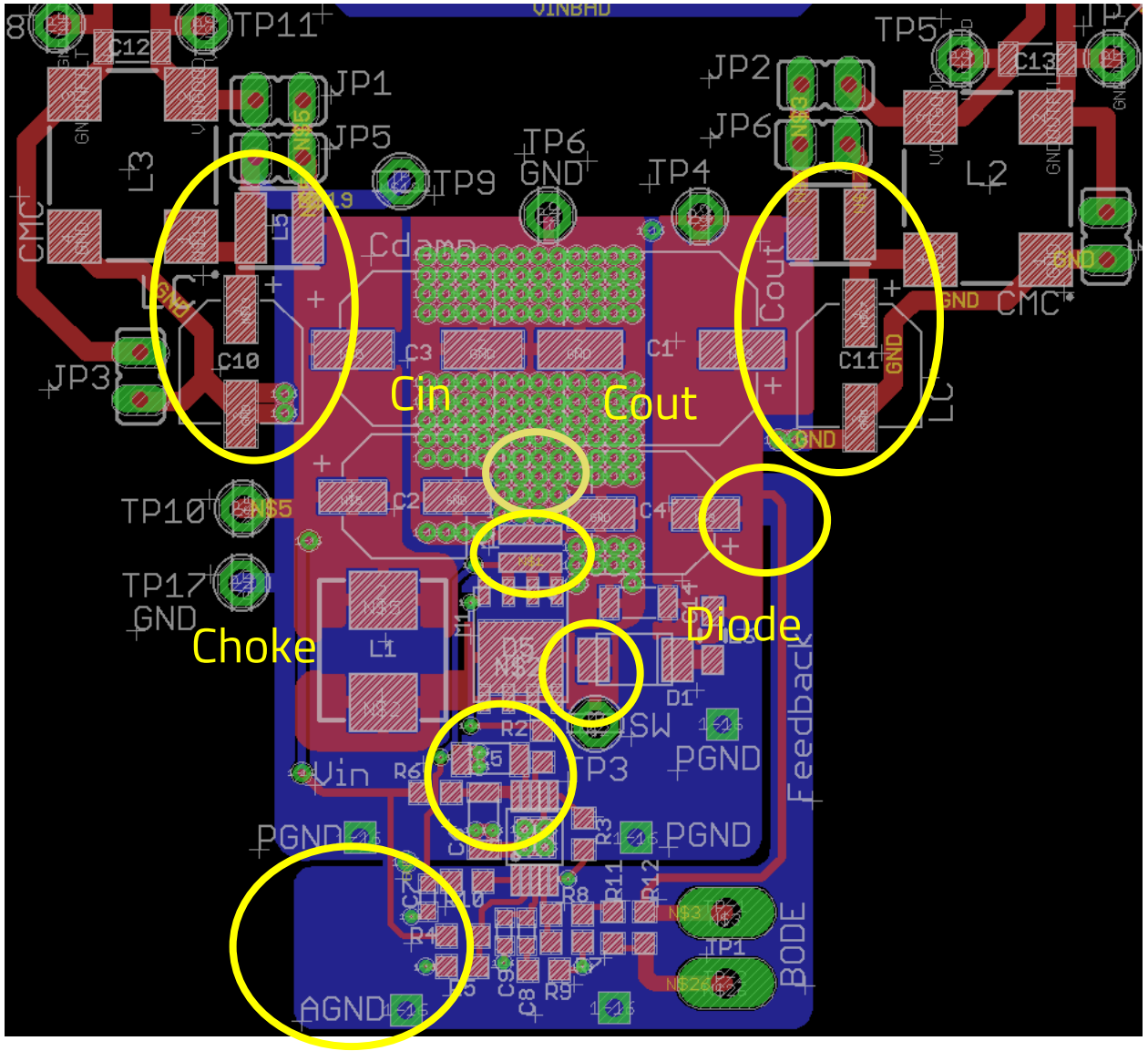


Schematic Good Design

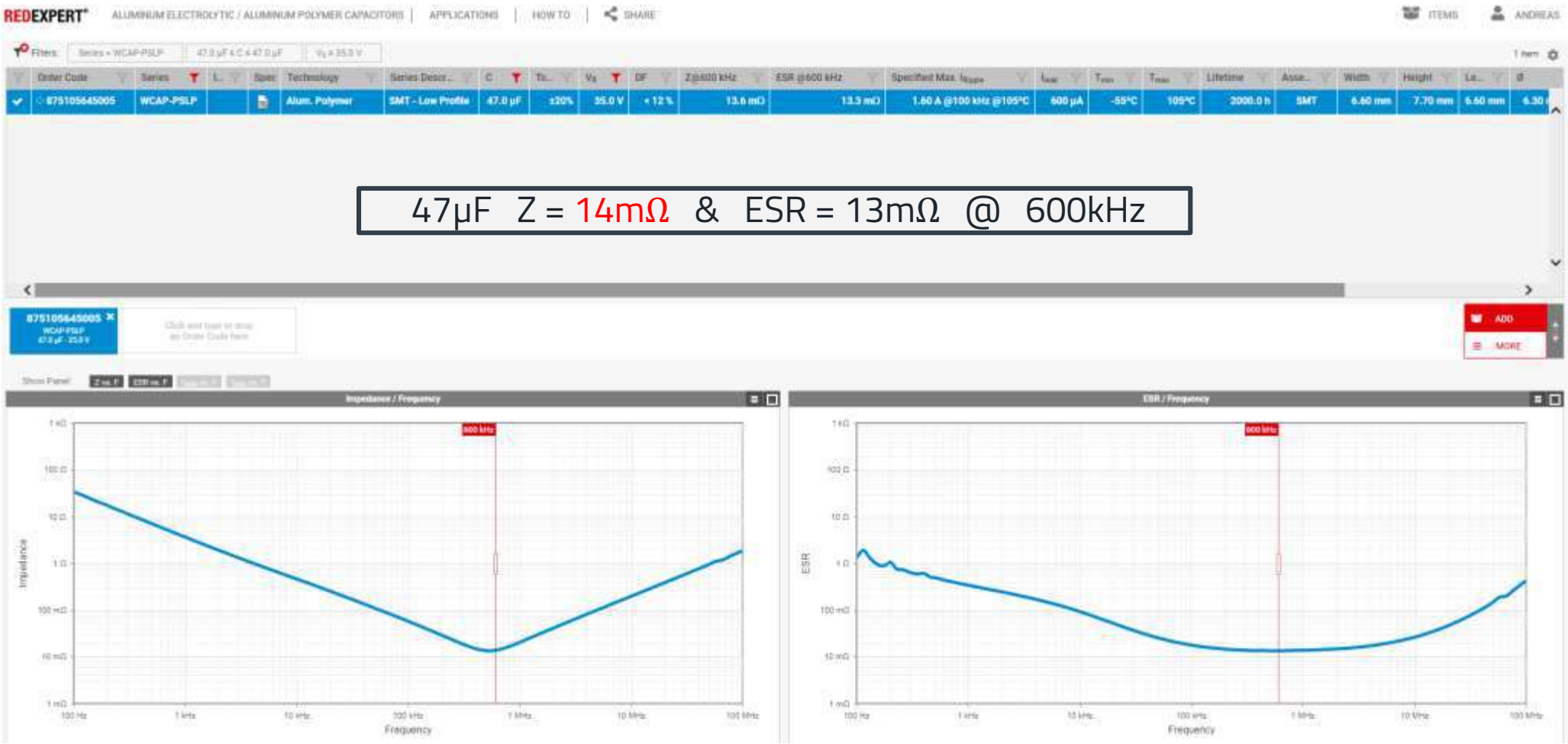
19V → 24V/0,5A



PCB Layout Good Design



Redexpert Polymer Cap Selection for Fsw 600kHz



Conducted EMI Calculation with 47µF Polymer Cin

Triangular approximation(differential mode only):

$$D = \frac{U_{out} - U_{in} + U_d}{U_{out} + U_d} = \frac{24V - 19V + 0{,}5V}{24V + 0{,}5V} = 0{,}224$$

$$\Delta I = \frac{U_{in}}{L \cdot f_{sw}} \cdot D = \frac{19V}{33\mu H \cdot 600kHz} \cdot 0{,}224 = 0{,}21A$$

$$|I_{cin}[600kHz]| = \frac{\Delta I}{\sqrt{2} \cdot \pi^2 \cdot D \cdot (1 - D)} \cdot |\sin(\pi \cdot D)| = \frac{0{,}21A}{\sqrt{2} \cdot \pi^2 \cdot 0{,}224 \cdot (1 - 0{,}224)} \cdot |\sin(\pi \cdot 0{,}224)| = 56mA$$

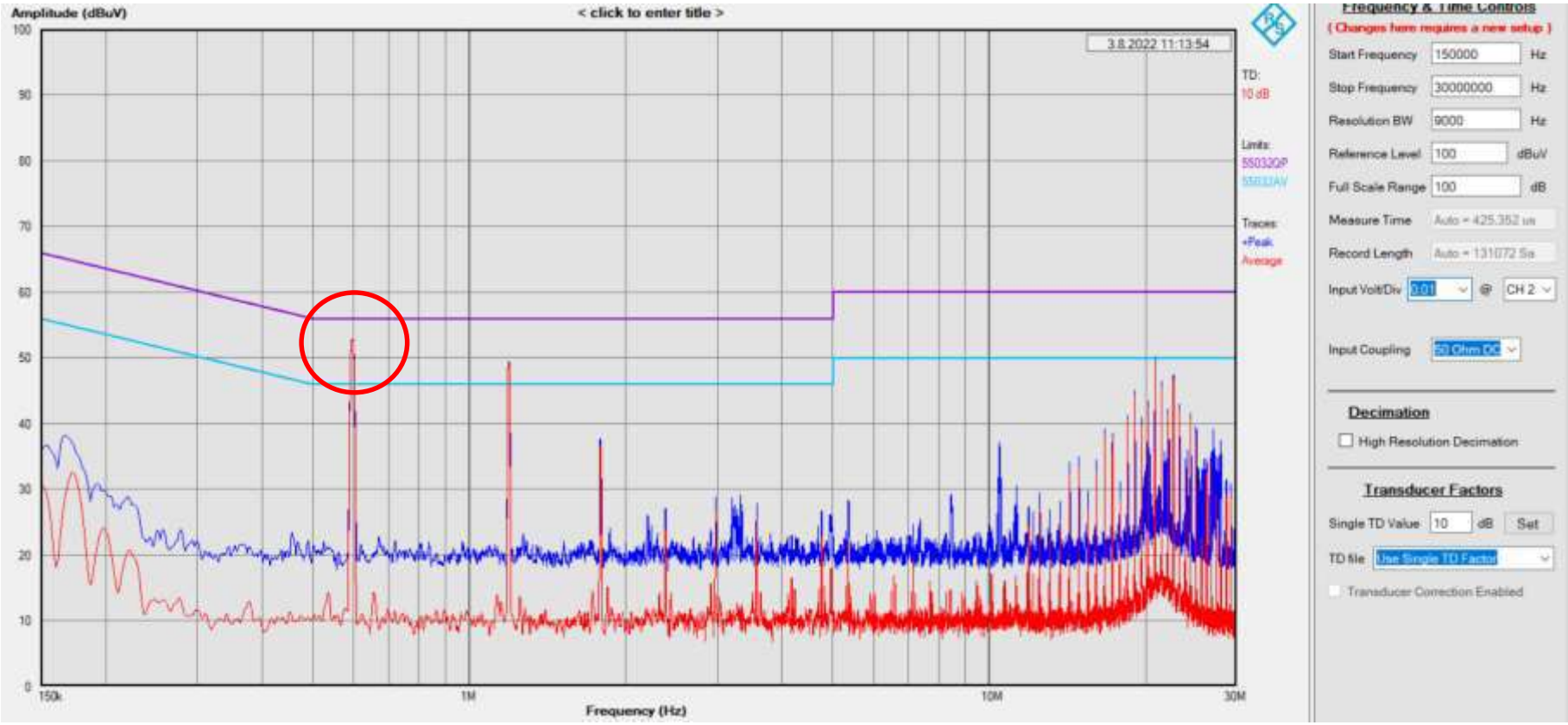
$$|U_{cin}(600kHz)| = |Z_{cin}(600kHz)| \cdot |I_{cin}(600kHz)| = 14m\Omega \cdot 56mA = 784\mu V$$

$$784\mu V \rightarrow 20\log\left(\frac{784\mu V}{1\mu V}\right) = 57{,}9dB\mu V - 6dB\mu V(LISN\ Voltage\ Divider) = 51{,}9dB\mu V$$

Limit CISPR32 Class B is 46dBµV → approx. 15dB Damping is necessary

Verification of the triangular approximation GOOD Design

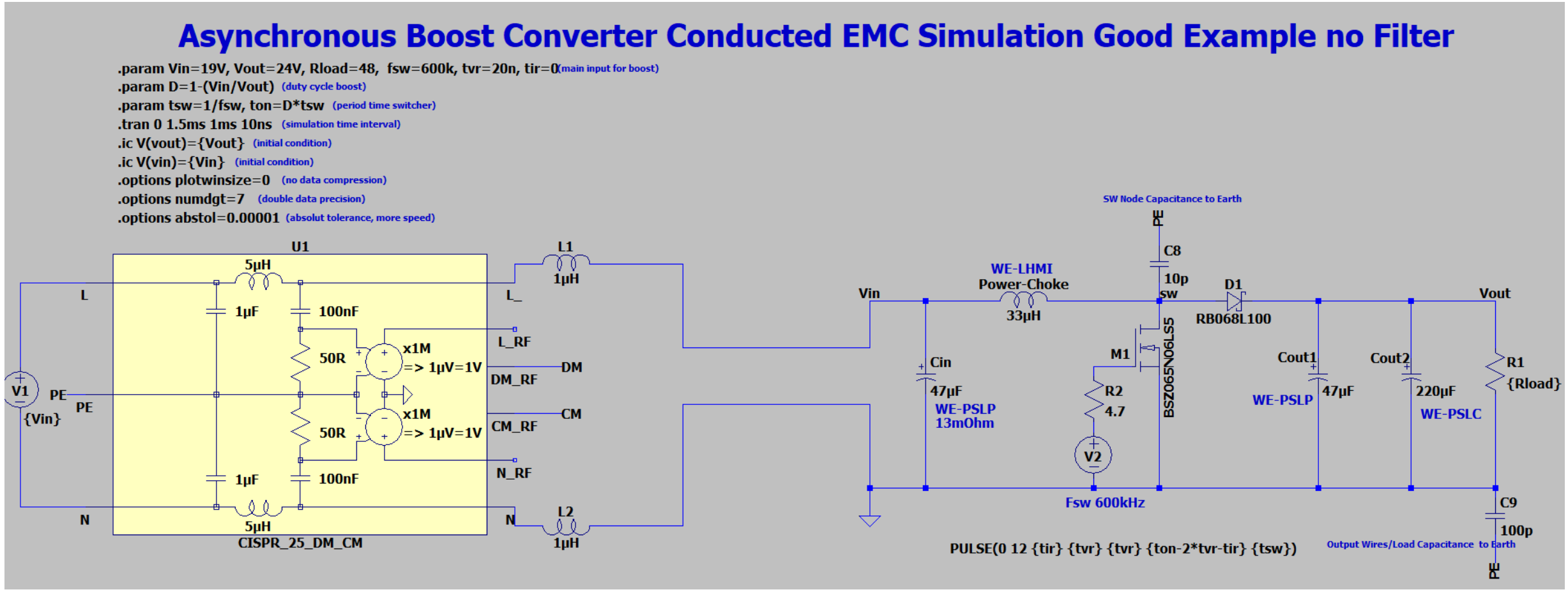
DM noise on input



52dBµV as calculated

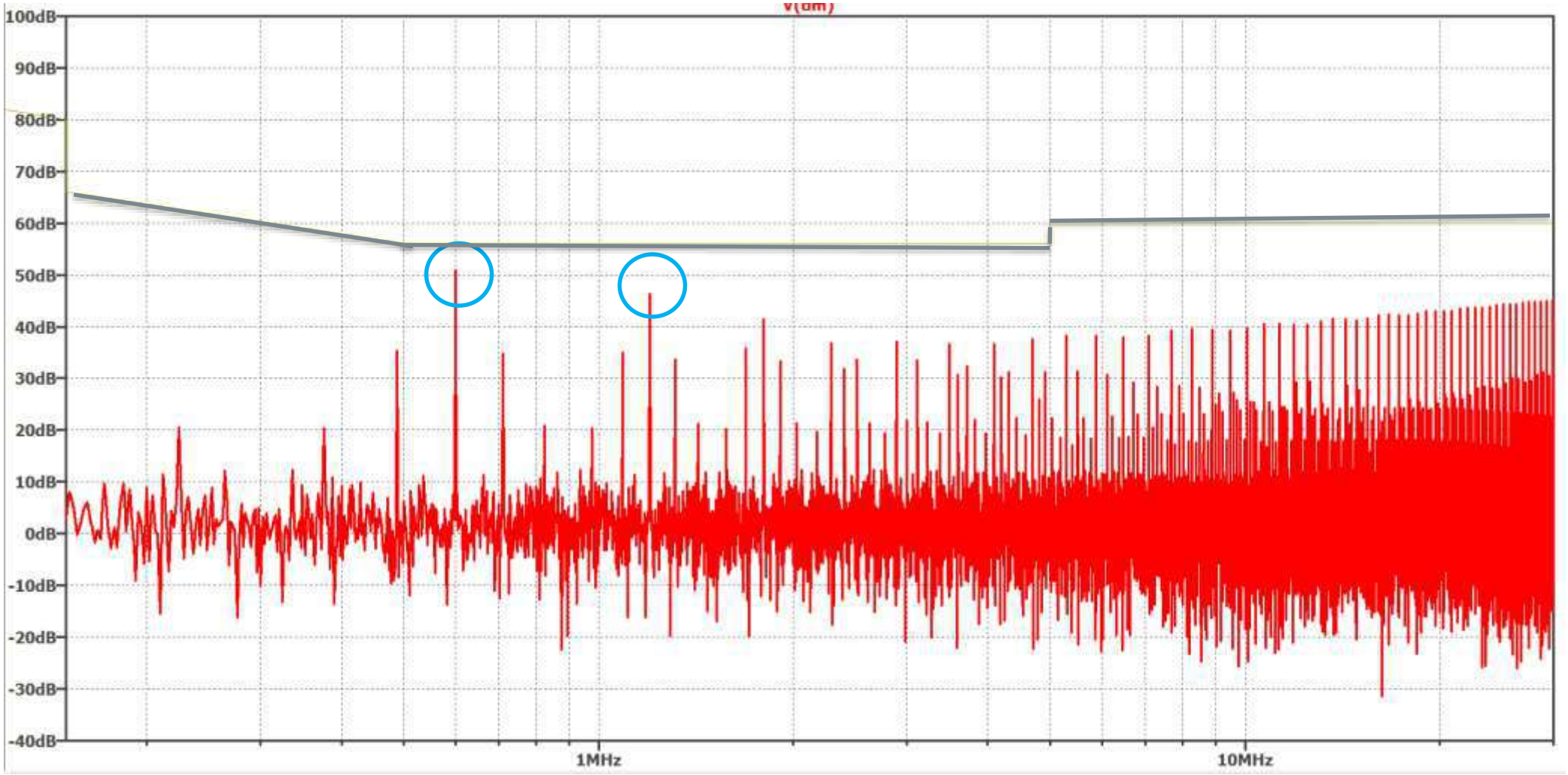
LT Spice Boost GOOD Simulation

Simple Model to double check the calculation



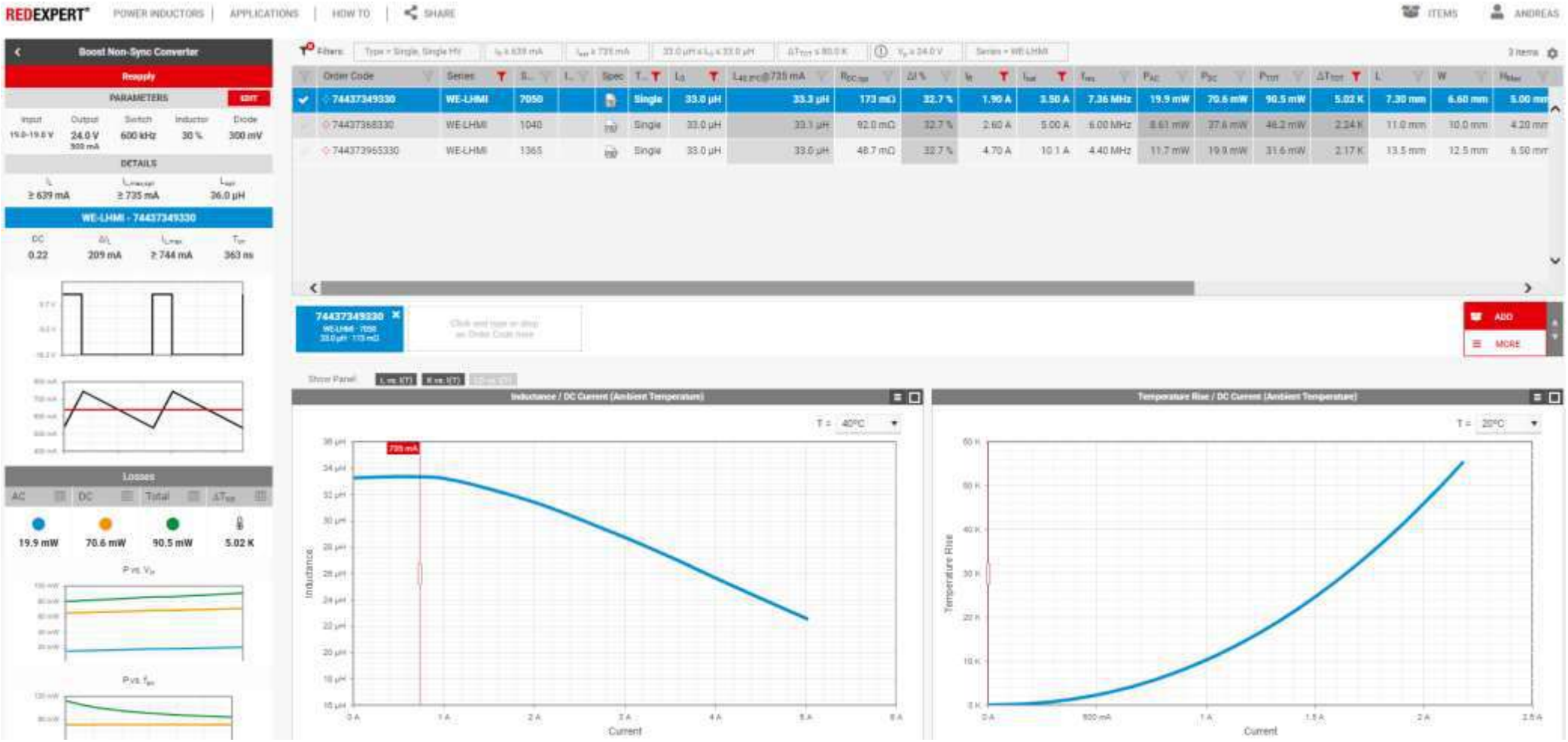
Simulated DM Noise with LT Spice

FFT Plot of the LISN DM Channel



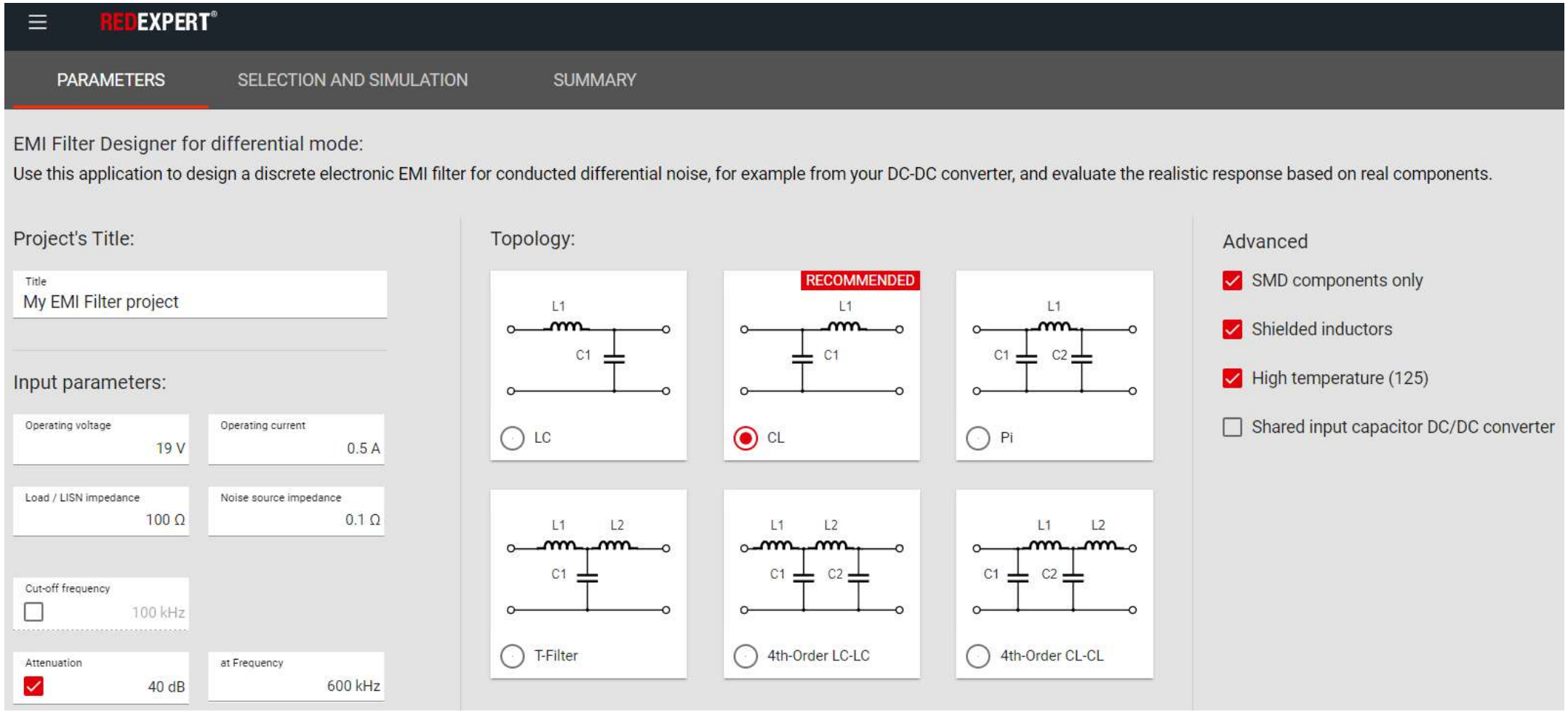
Redexpert Power Inductor Selection

Fully shielded high performance inductor WE-LHMI



Filter Simulation Redexpert

Designing an DCDC input filter



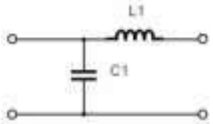
Filter Simulation Redexpert Summary

Good choice to filter the range from 150kHz to 30MHz

REDEXPERT® Filter Designer

PARAMETERS | SELECTION AND SIMULATION | SUMMARY

Circuit Schematic



Specifications

Edit

"My EMI Filter project"

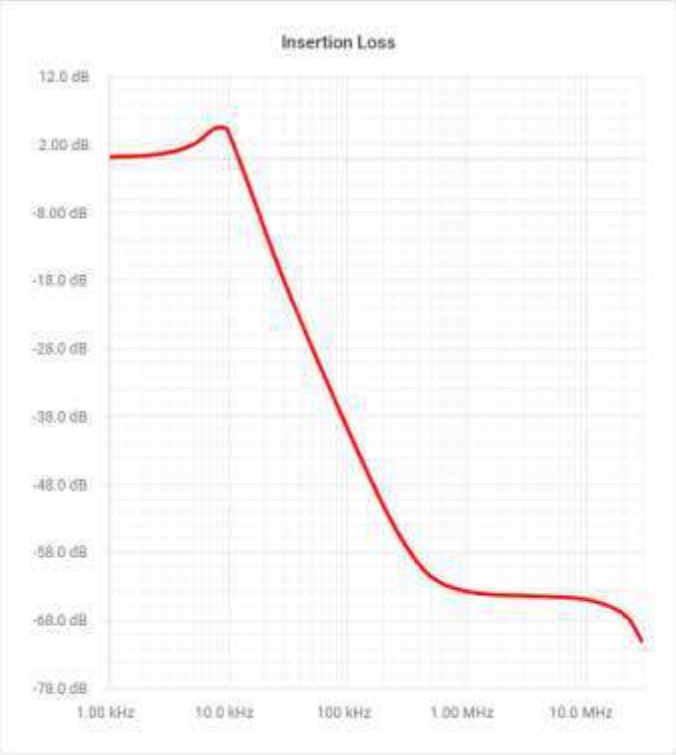
TYPE: CL
V_{op}: 19.0 V
I_{op}: 500 mA
LOAD / LISN IMPEDANCE: 100 Ω
NOISE SOURCE IMPEDANCE: 100 mΩ
ILOSS -62.5 dB@600 kHz

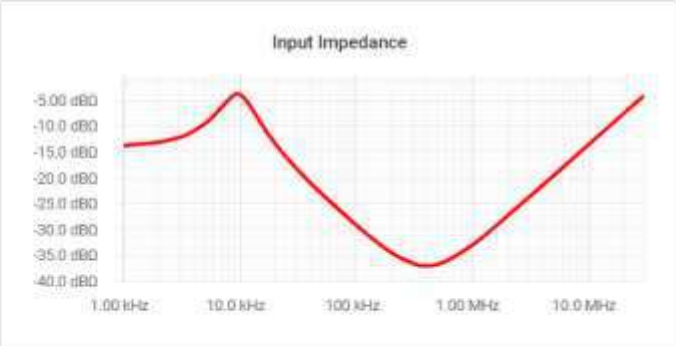
Bill Of Materials

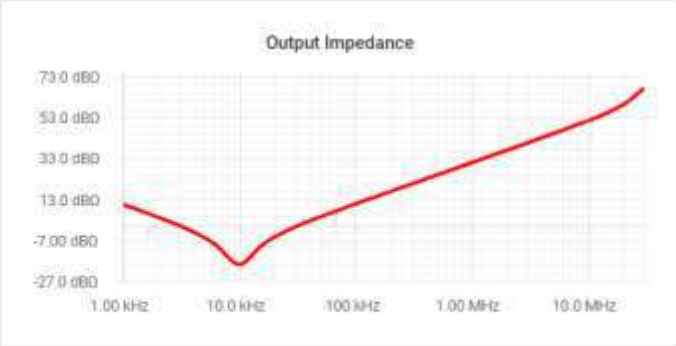
ADD

#	Na...	Order Code	Value	Properties	Qty
1.	C1	875105645005	47.0 µF	Assembling Technology = SMT Capacitance = 47.0 µF Rated Voltage = 35.0 V Height = 7.70 mm	1
2.	L1	74404042068	6.80 µH	Inductance = 6.80 µH Rated Current = 1.45 A Type = Single	1

Simulation Responses

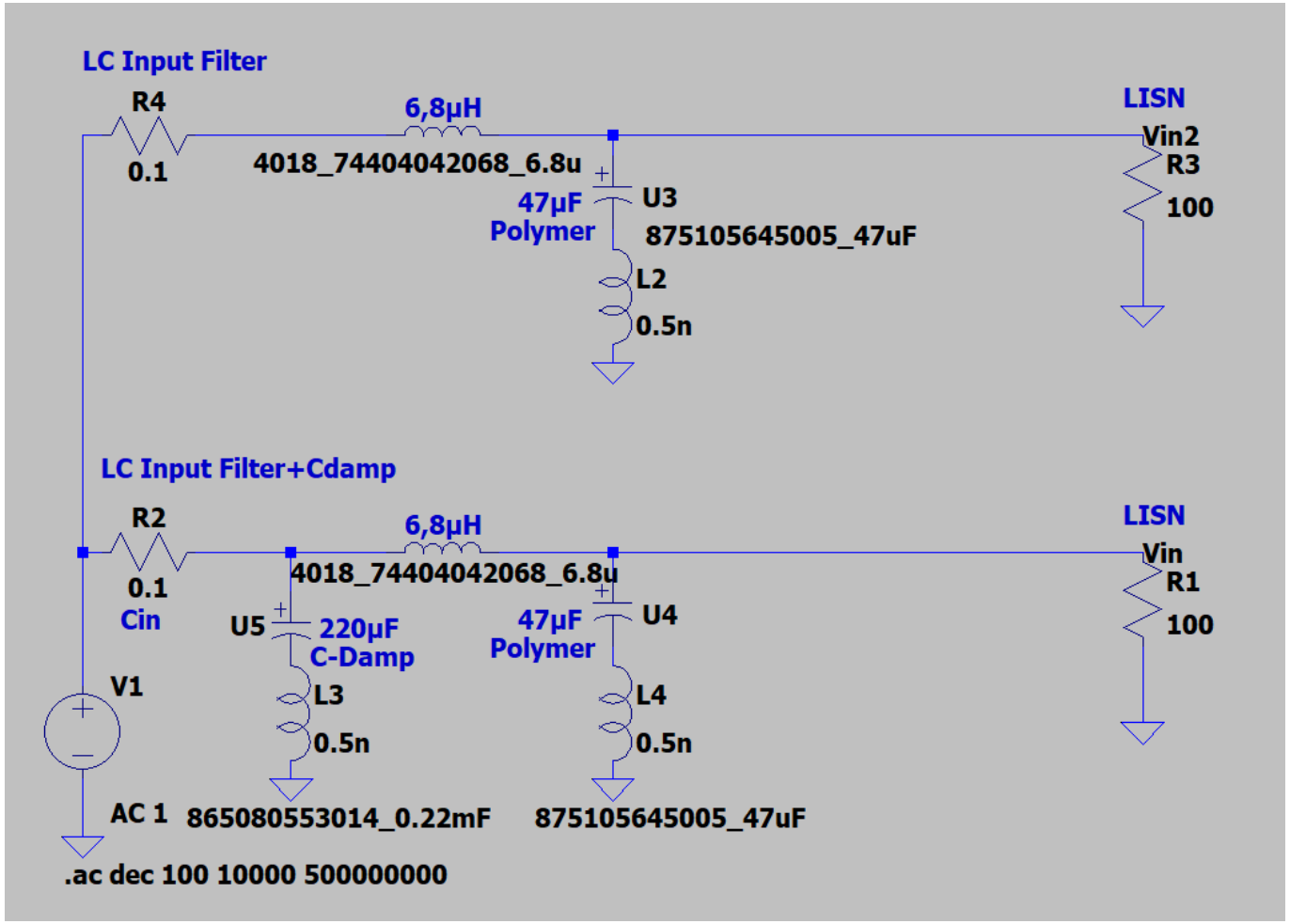






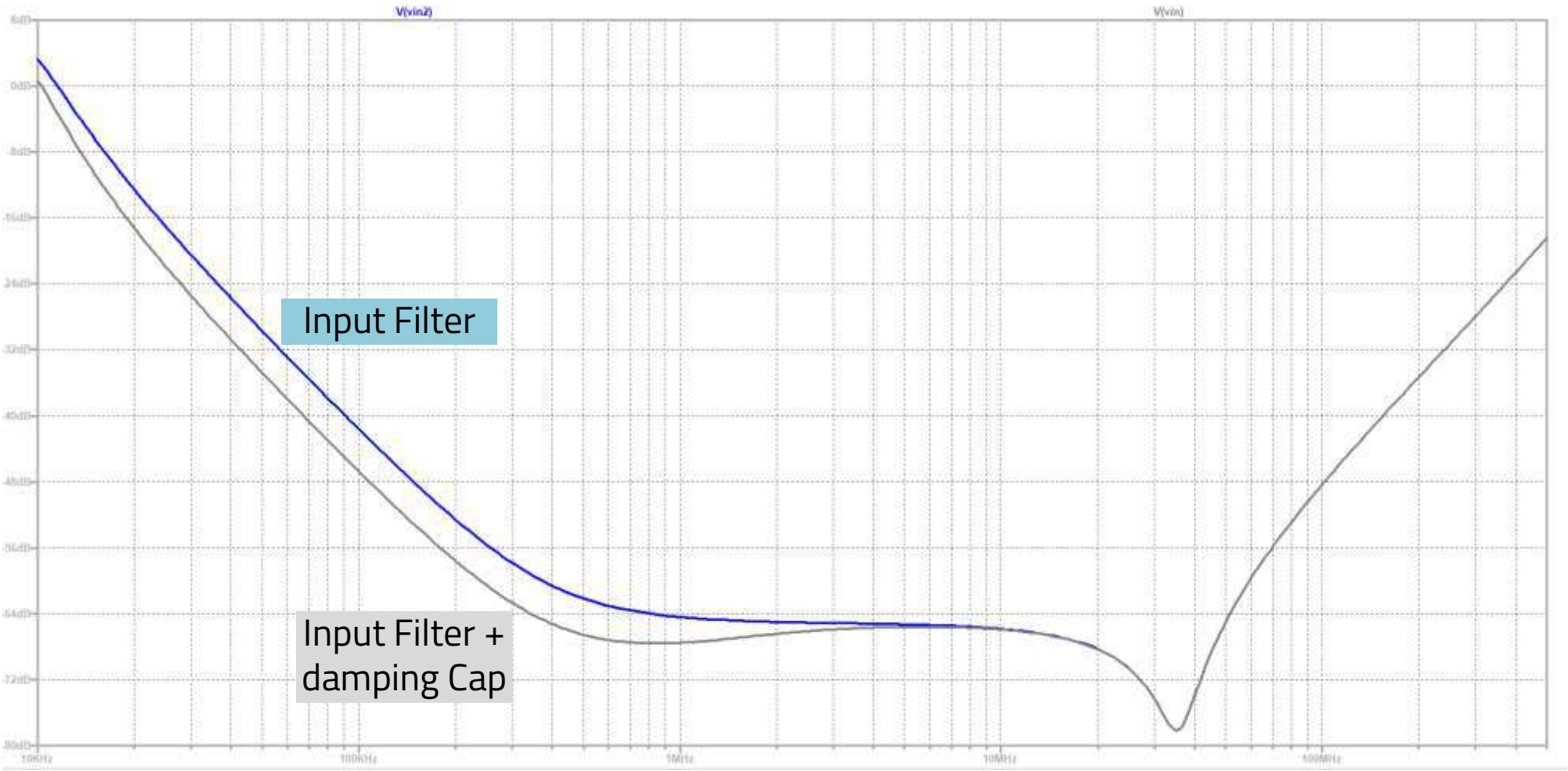
Filter Simulation Differential Mode in LT Spice

LC Filter with/without damping Cap + GND Vias



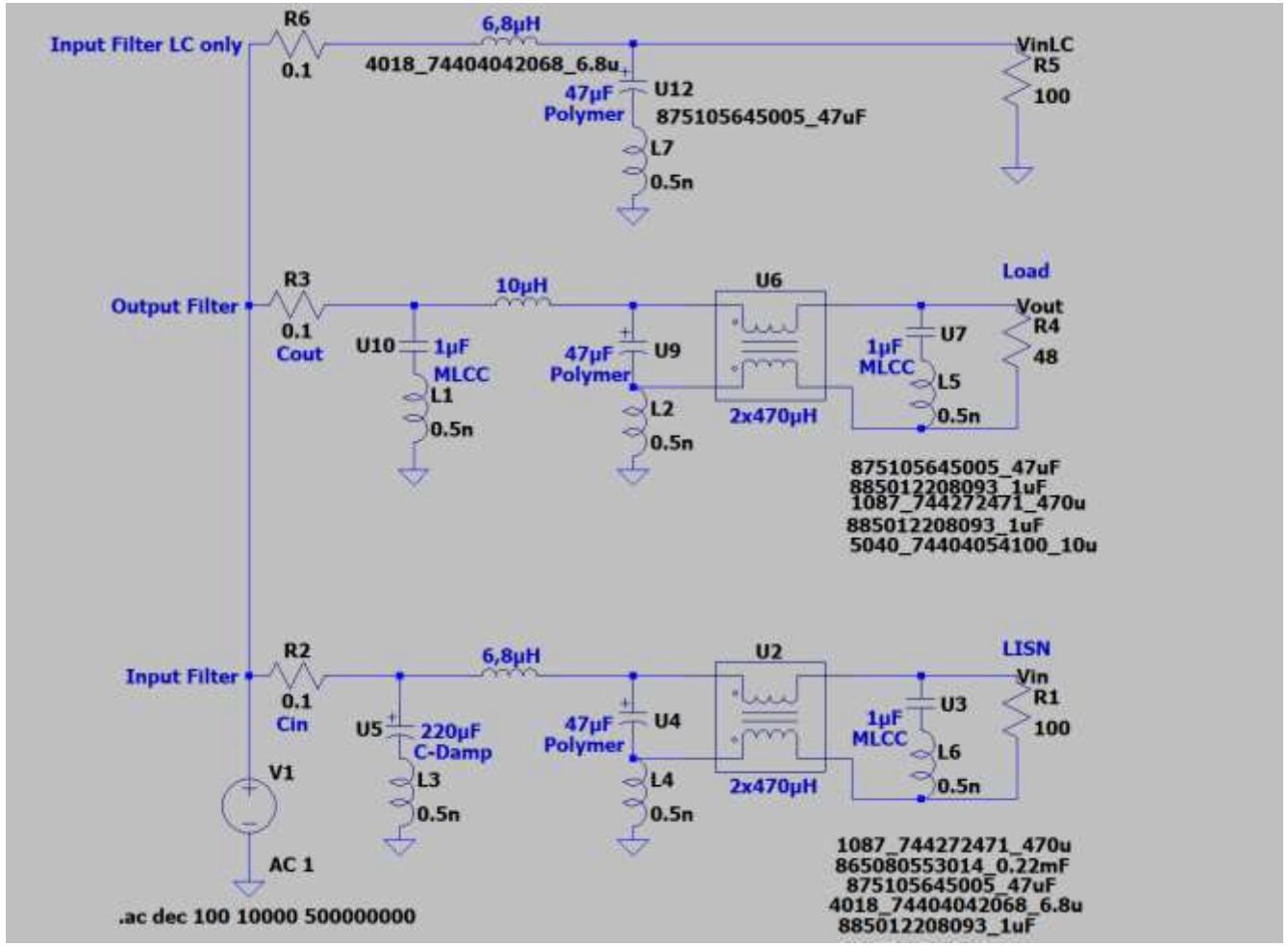
Filter Simulation Differential Mode in LT Spice

LC Filter with/without damping Cap + GND Vias



Filter Simulation Differential Mode in LT Spice

All filter components on input & output + GND Vias



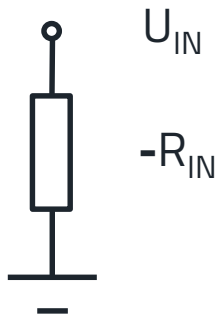
Filter Simulation Differential Mode in LT Spice

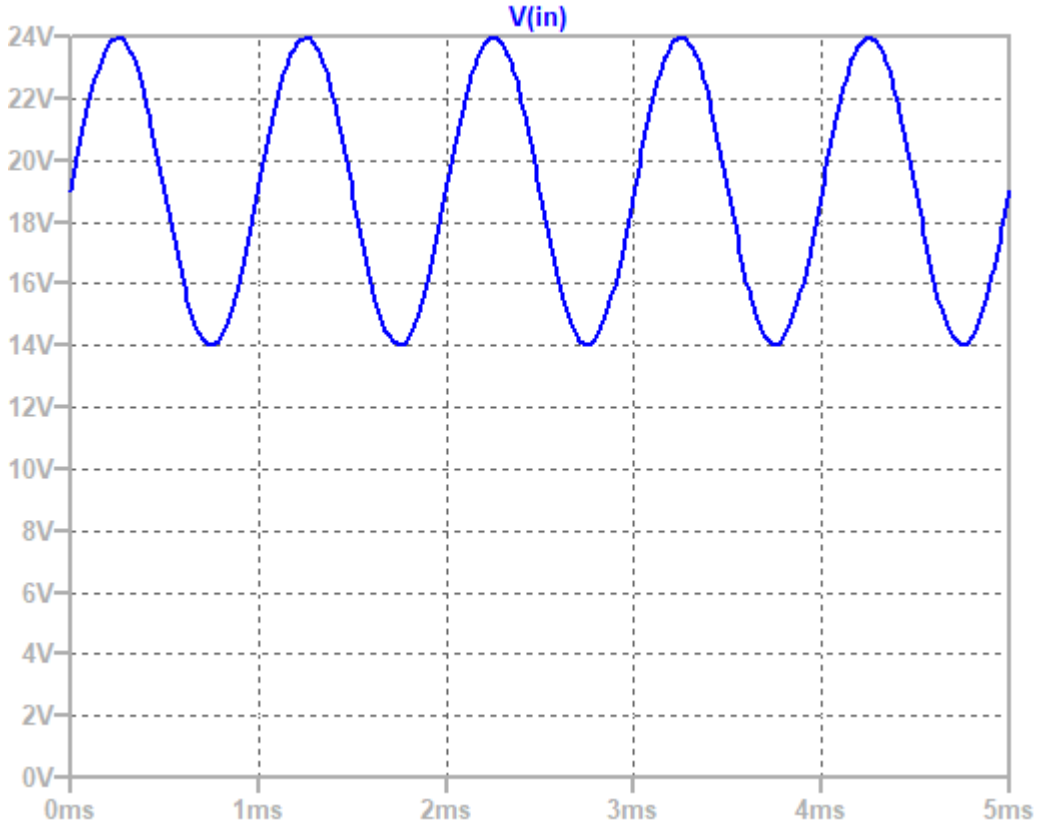
All filter components on input & output + GND Vias

Why is Inputfilter damping maybe necessary?

- The input capacitor is part of the input filter and forms an oscillating circuit together with the filter choke and/or the line inductance

- A regulated DC/DC converter behaves like a "negative" resistor at the input:
  - $P_{IN} \sim P_{OUT} = \text{const.}$
    $\rightarrow V_{IN}\uparrow \rightarrow I_{IN}\downarrow \rightarrow V_{IN}\downarrow \rightarrow I_{IN}\uparrow$





Why is Inputfilter damping maybe necessary?

theoretical background

- Correction factor in the loop gain of the control loop due to the input filter:
  - Middlebrook's Extra-Element Theorem

$$\mathbf{H(s)} = \boldsymbol{H}_{\mathbf{Z_{OUT}=0}}(\boldsymbol{s}) \cdot \left(\frac{\mathbf{1} + \frac{\mathbf{Z_{OUT}}}{\mathbf{Z_N}}}{\mathbf{1} + \frac{\mathbf{Z_{OUT}}}{\mathbf{Z_D}}} \right)$$

Goal $\rightarrow \left(\frac{1+\frac{Z_{OUT}}{Z_N}}{1+\frac{Z_{OUT}}{Z_D}} \right) \approx 1 = 0\mathrm{dB}$

$\rightarrow \mathbf{Z_{OUT}} \ll \mathbf{Z_N}$ and $\mathbf{Z_{OUT}} < \mathbf{Z_D}$

rule of thumb: $\mathbf{Z_{OUT}}$ < 1/10th of $\mathbf{Z_N}$

where:

H (s):
transfer function with filter

$H_{ZOUT=0}$ (s):
transfer function without filter

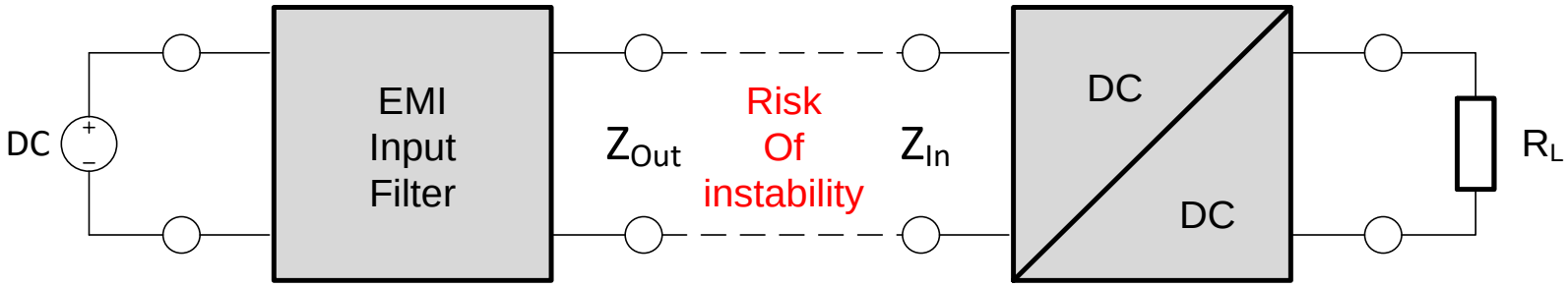
Z_{OUT}:
Output impedance of the LC filter

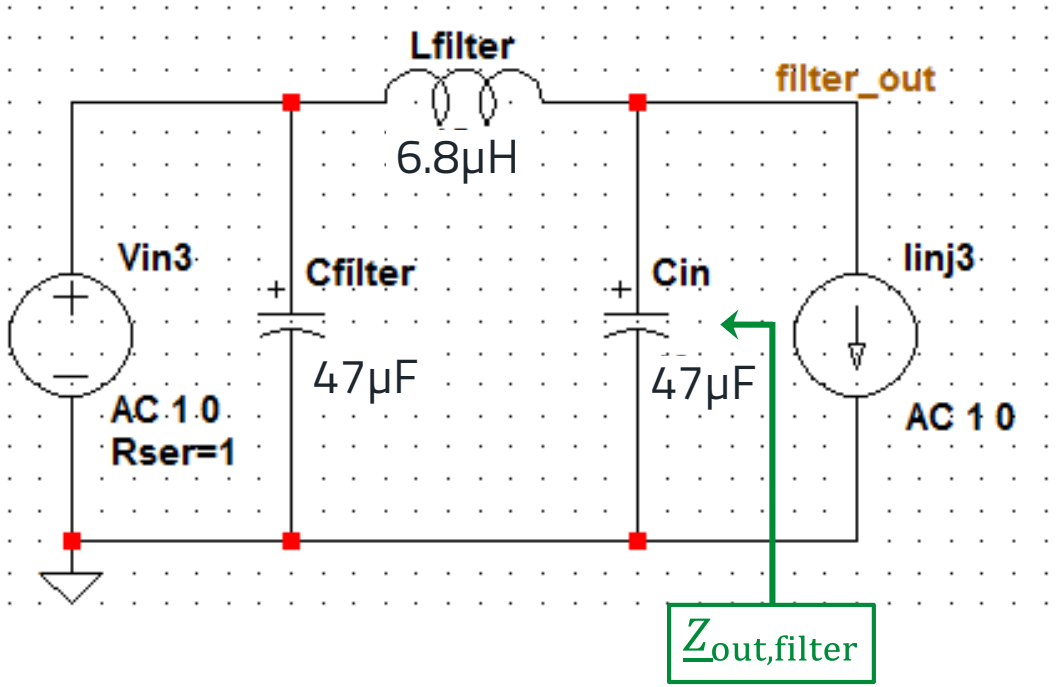
Z_N:
Input impedance of the converter with constant output voltage (static input impedance)

Z_D:
Input impedance of the converter with a constant duty cycle (open loop input impedance)

Why is Inputfilter damping maybe necessary?

Output impedance of input filter must be lower than DCDC input impedance over a certain frequency range



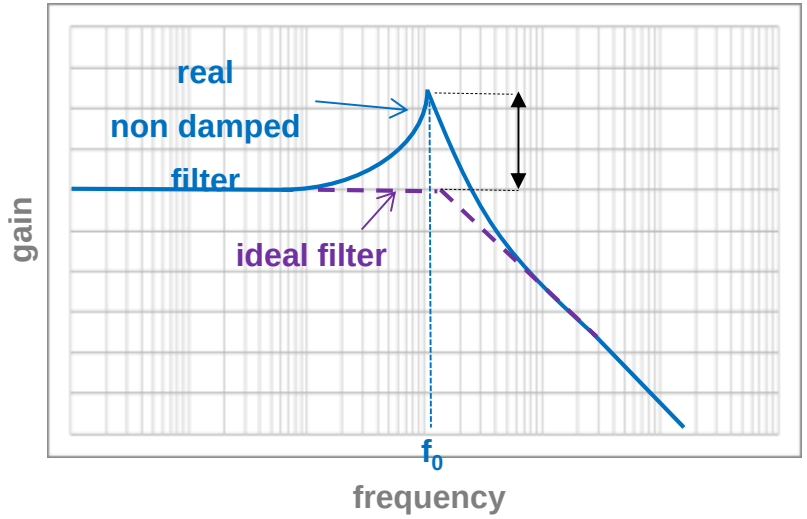


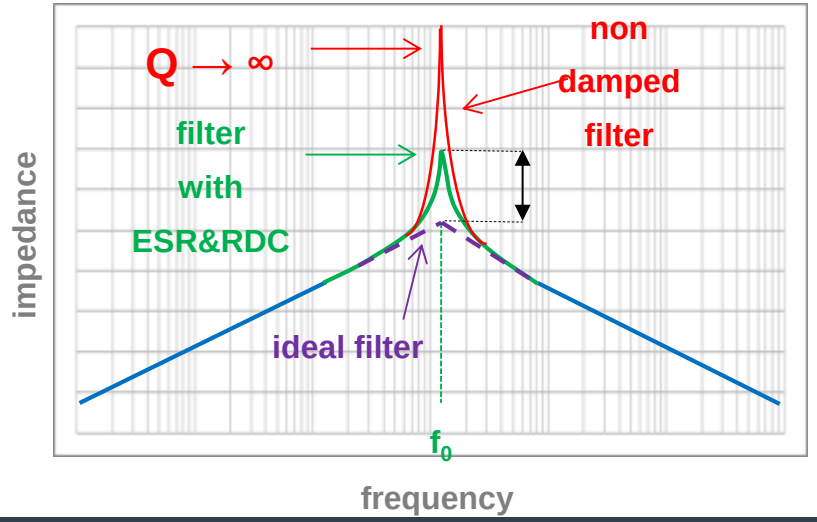
→ DCDC input impdance

Influence of Lf + Cin

The filter inductor forms with Cin a impedance overshoot at the corner frequency of this LC filter

- L_filter & Cin (not C_filter!!)form a resonance overshoot at f0
- Resonance overshoots are caused by parasitic component effects
- ESR and RDC of C and L reduce these peaks
- Magnitude depends on Q
- Filter output impedance is highest at f0
- If the output impedance of the LC filter exceeds the input impedance of the converter, the system becomes unstable



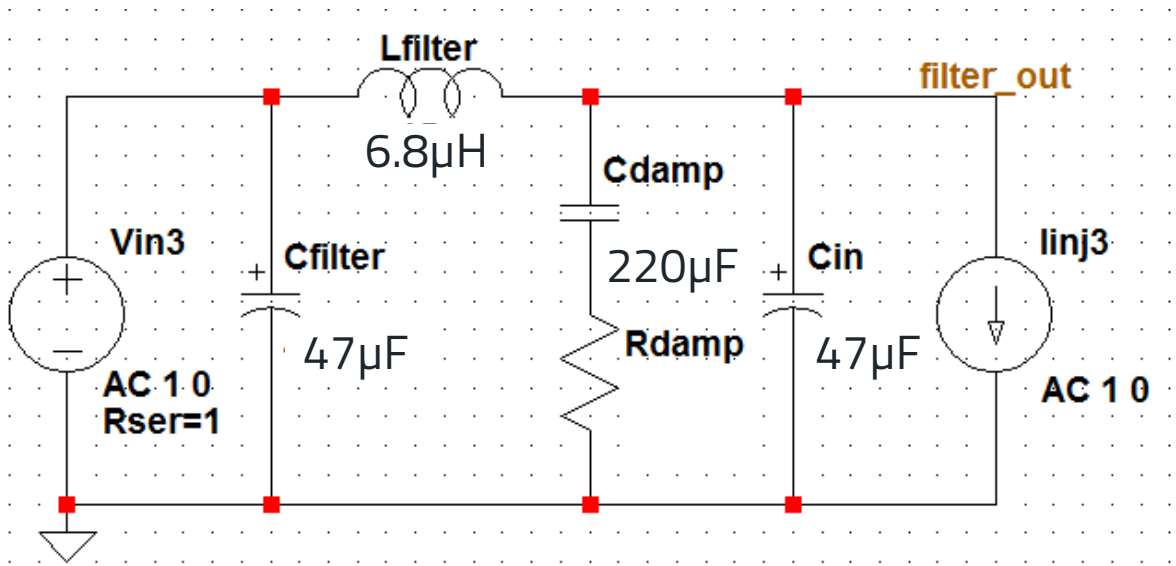


Damping of the Impedance Peak at LC Corner frequency

Calculate the required damping capacitor and resistor (or ESR)

$$n = 4\ (good\ starting\ point)\ \longrightarrow C_{damp} = 4 \cdot C_{in} = 4 \cdot 47\mu F = 188\mu F\ \longrightarrow \mathbf{220\mu F}\ chosen$$

$$R_{damp} = \sqrt{\frac{L_{filter}}{C_{in}}} = \sqrt{\frac{6{,}8\mu H}{47\mu F}} = 0.38\Omega$$



Choose Cdamp with Redexpert

Choose a cap between 150mΩ to 300mΩ ESR @ 8,9kHz corner frequency for propper damping

Order Code	Series	I...	Spec	Technology	Series Description	C...	To...	V_R	DF	Z@10.9 kHz	ESR @10.4 kHz	Maximum I_R	Specified Max. I_{Ripple}
865080553014	WCAP-ASLI			Alum. Electrolytic	SMT - Low Impedance +10...	220 µF	±20%	35.0 V	< 14 %	188 mΩ	166 mΩ	507 mA	570 mA @100 kHz @105

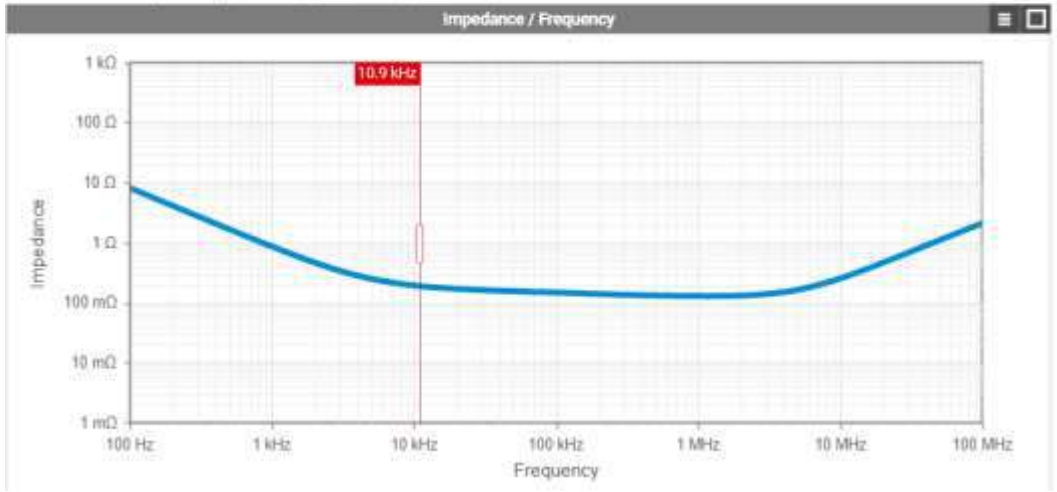
865080553014 ×
WCAP-ASLI
220 µF · 35.0 V

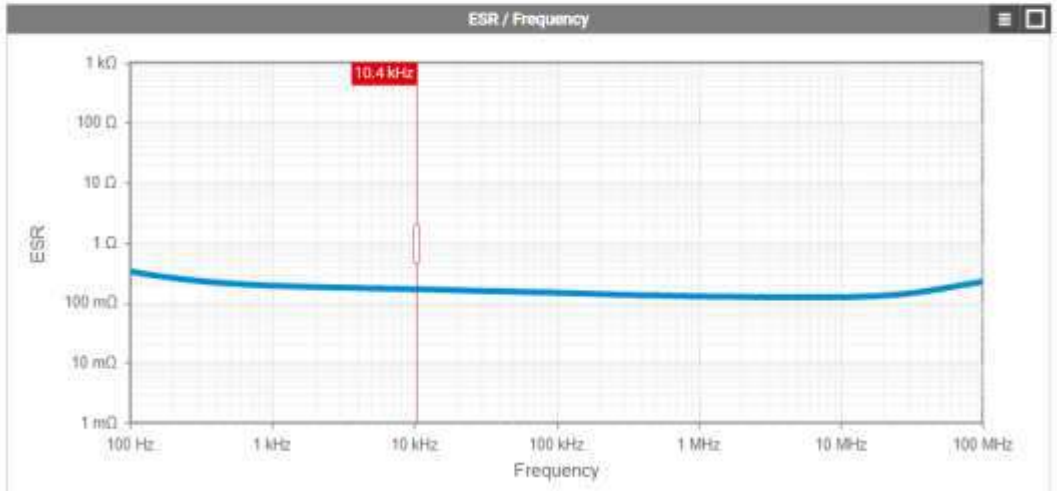
Click and type or drop an Order Code here

ADD

MORE

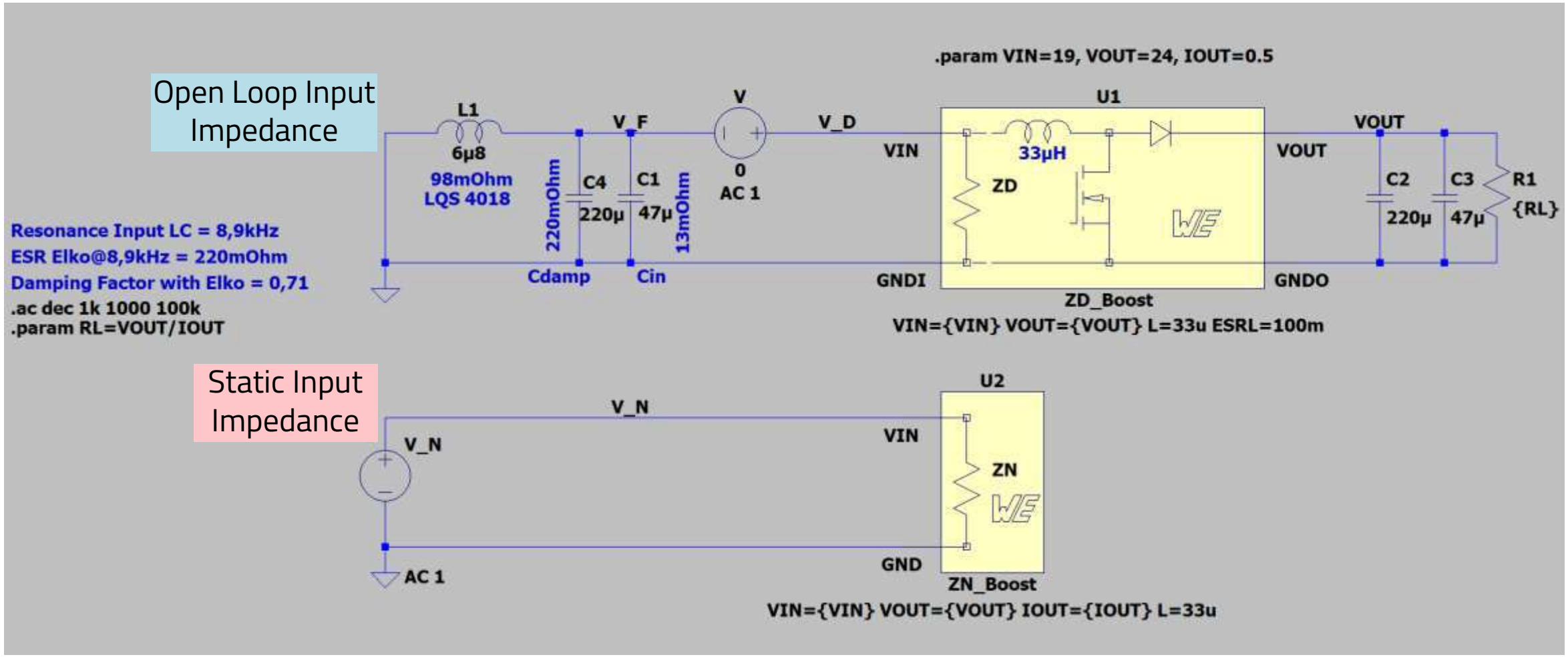
Show Panel: Z vs. F | ESR vs. F





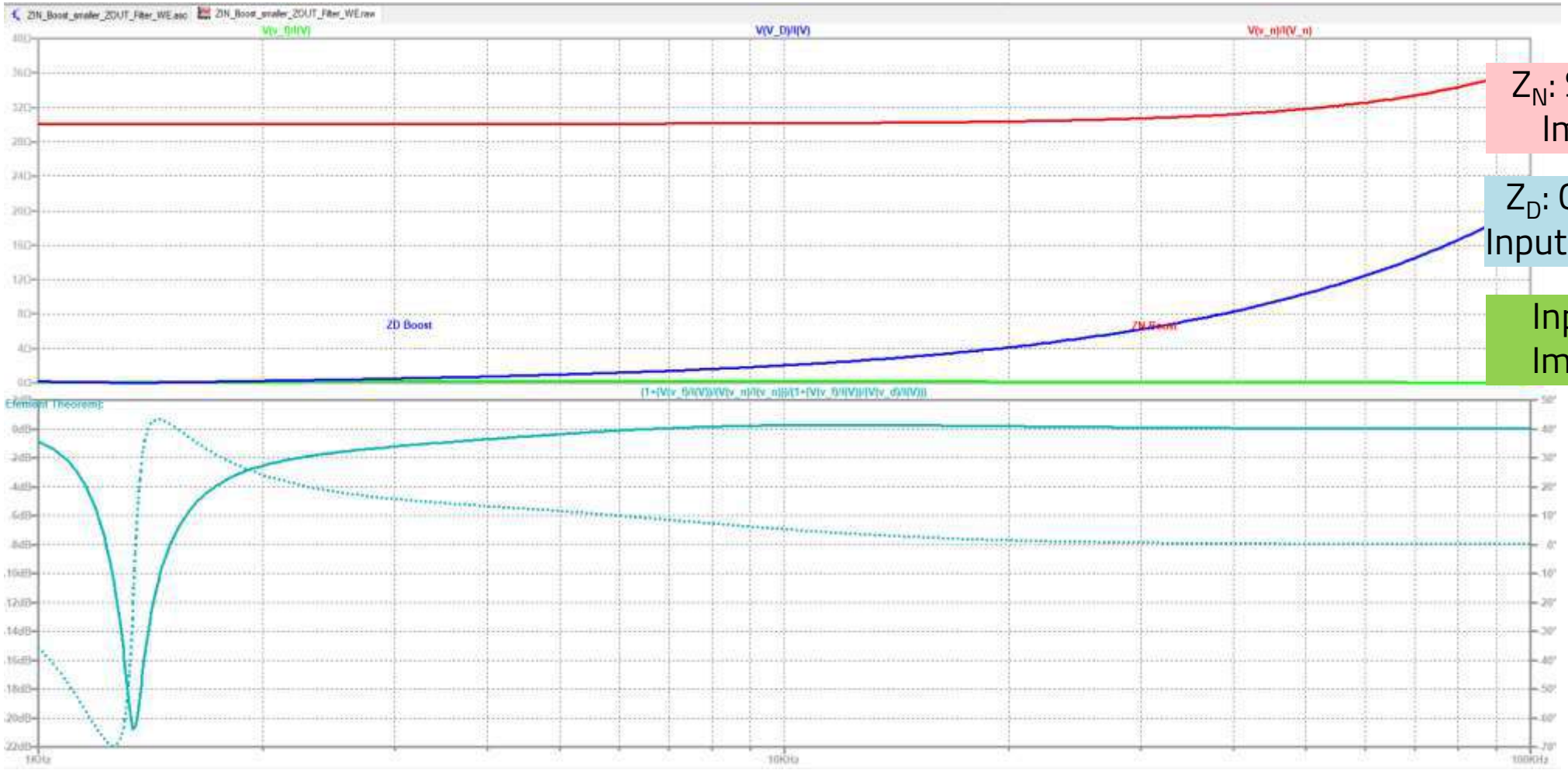
Input Filter Stability Simulation

With damping cap and 6,8µH filter choke



Input Filter Stability Simulation

With damping capacitor and 6,8µH filter choke



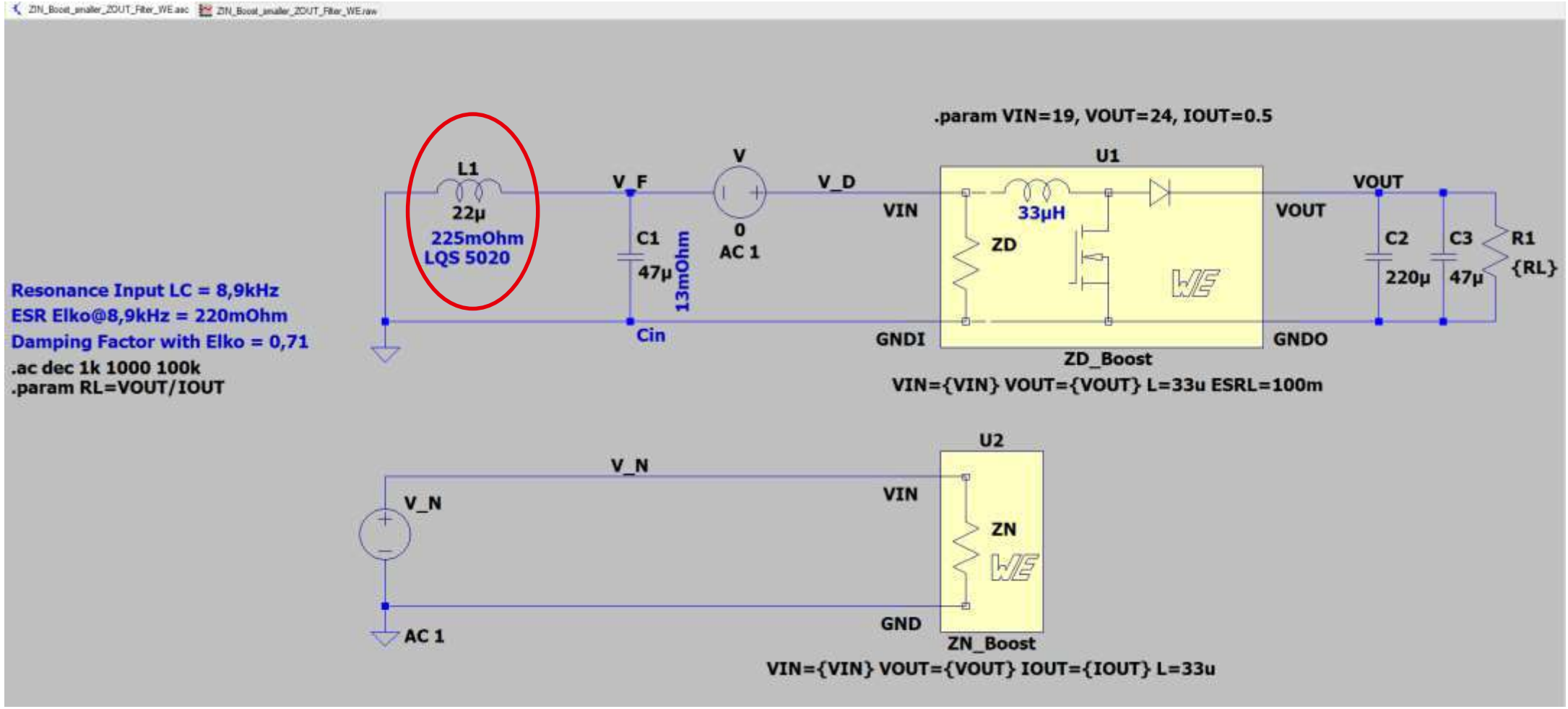
Z_N: Static Input Impedance

Z_D: Open Loop Input Impedance

Input Filter Impedance

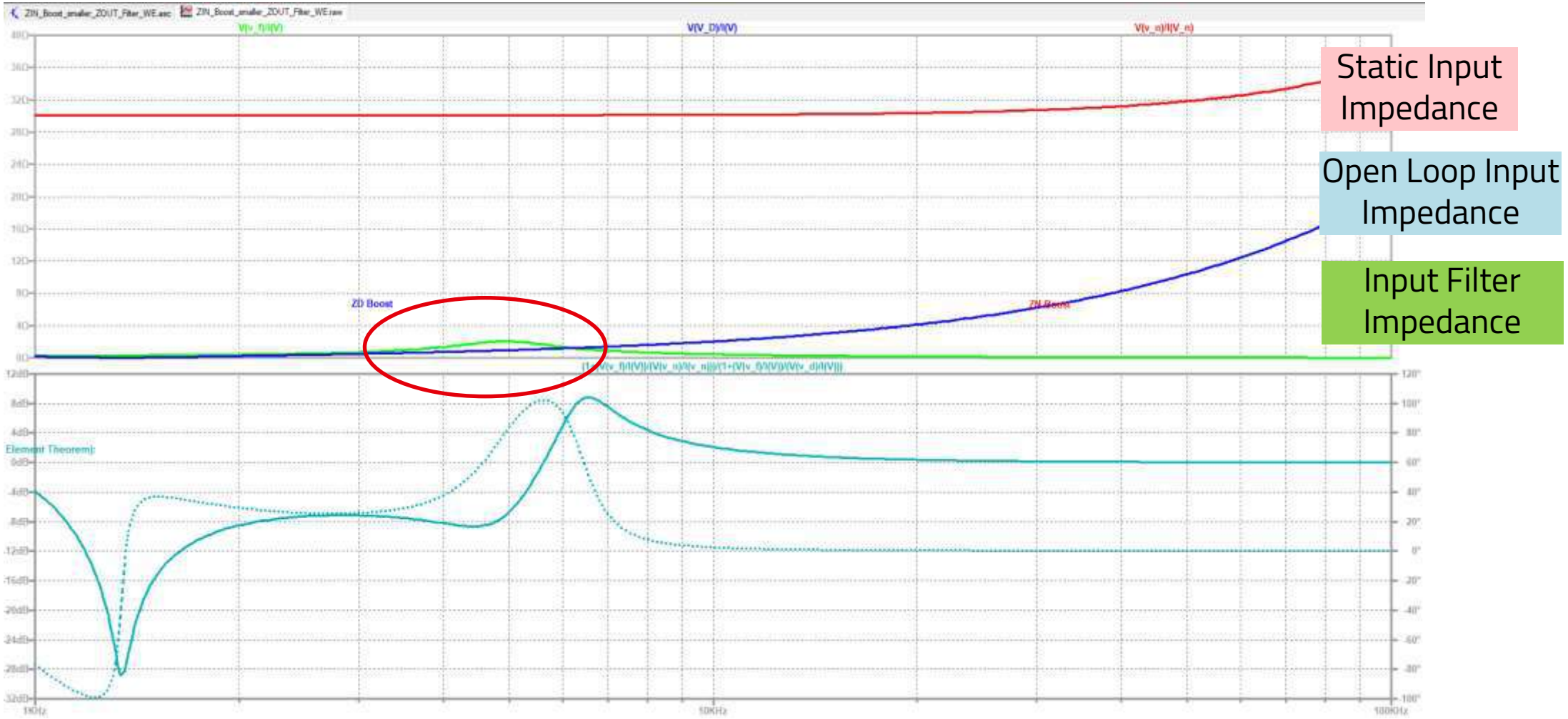
Input Filter Stability Simulation

No Damping capacitor and bigger filter inductance value of 22uH



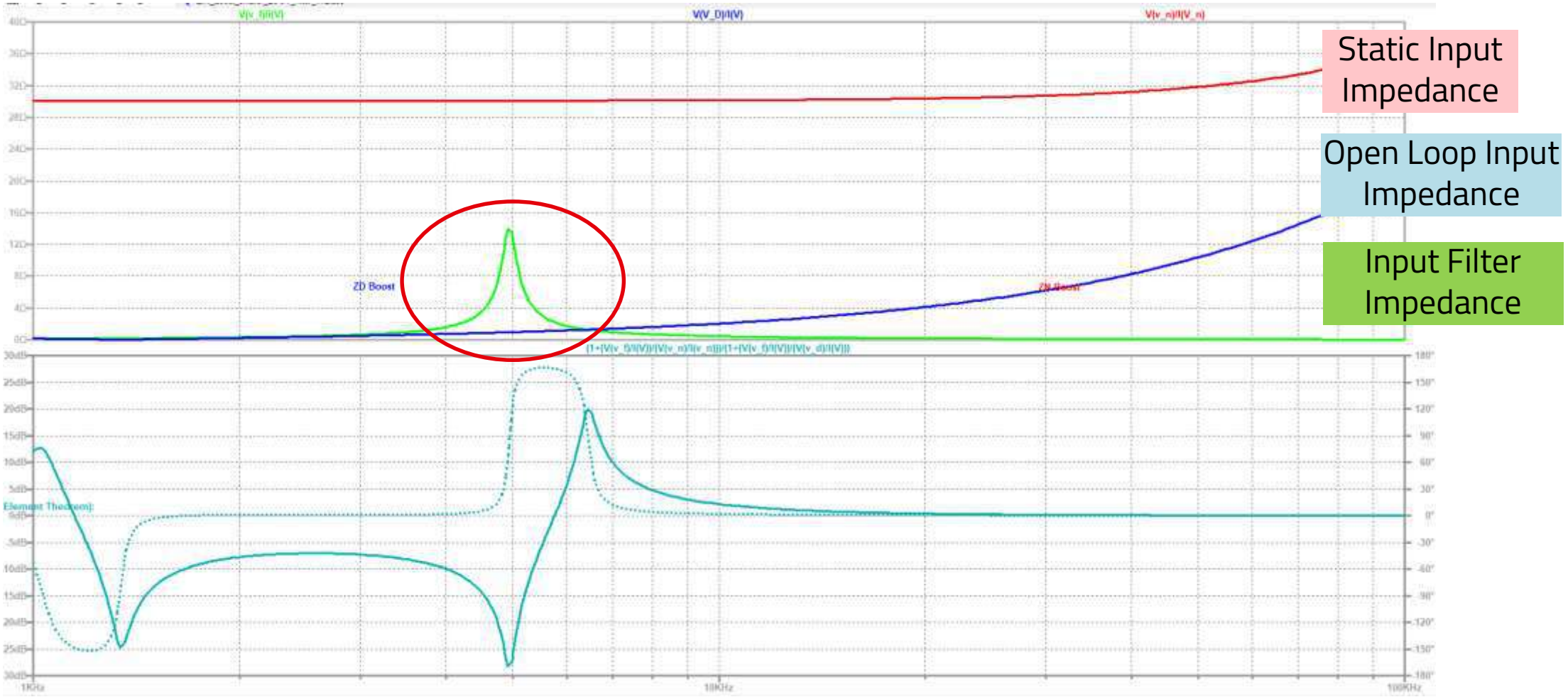
Input Filter Stability Simulation

No damping capacitor and bigger filter inductance value of **22uH/225mΩ(Rdc)**



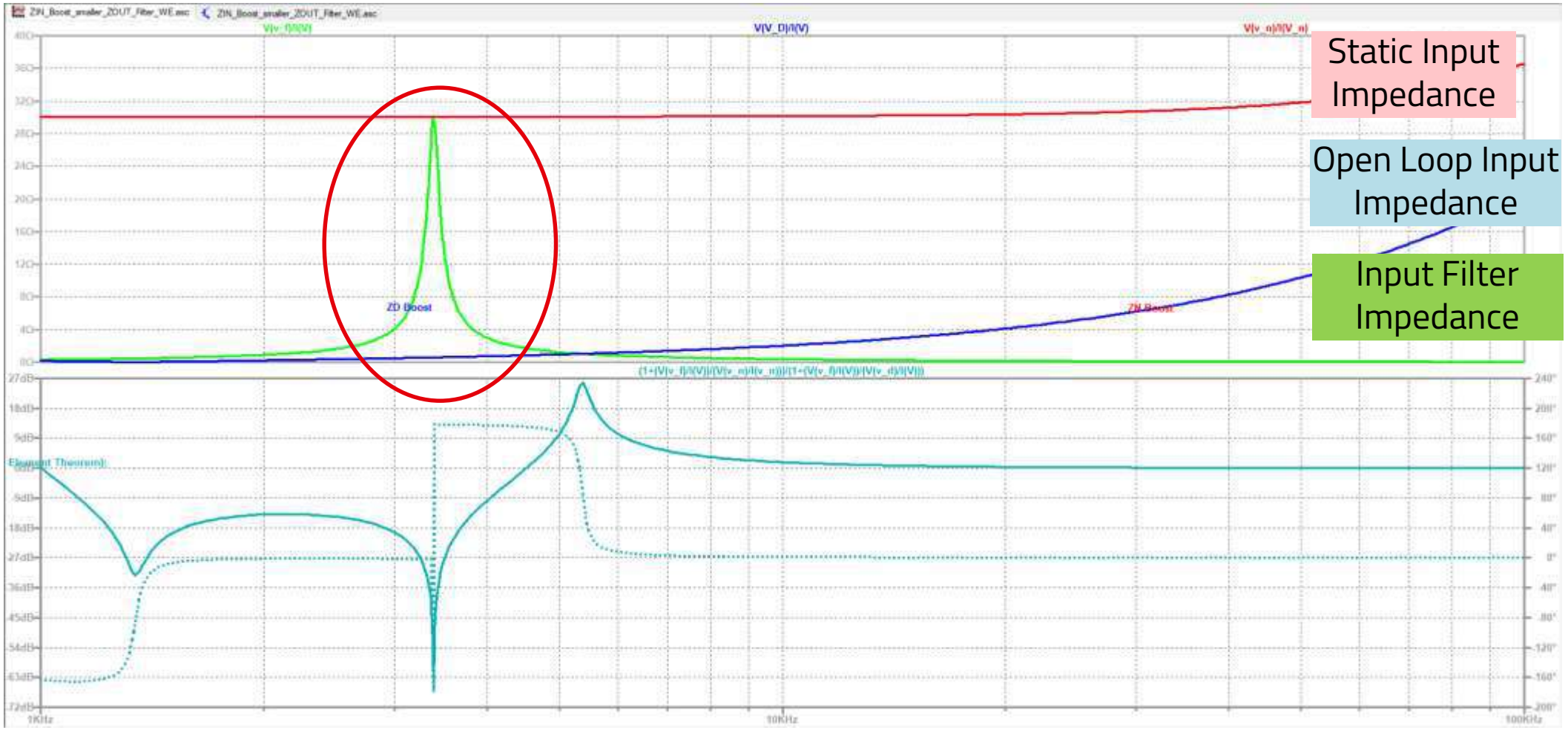
Input Filter Stability Simulation

No damping capacitor and bigger filter inductance value of **22uH/25mΩ(Rdc)**



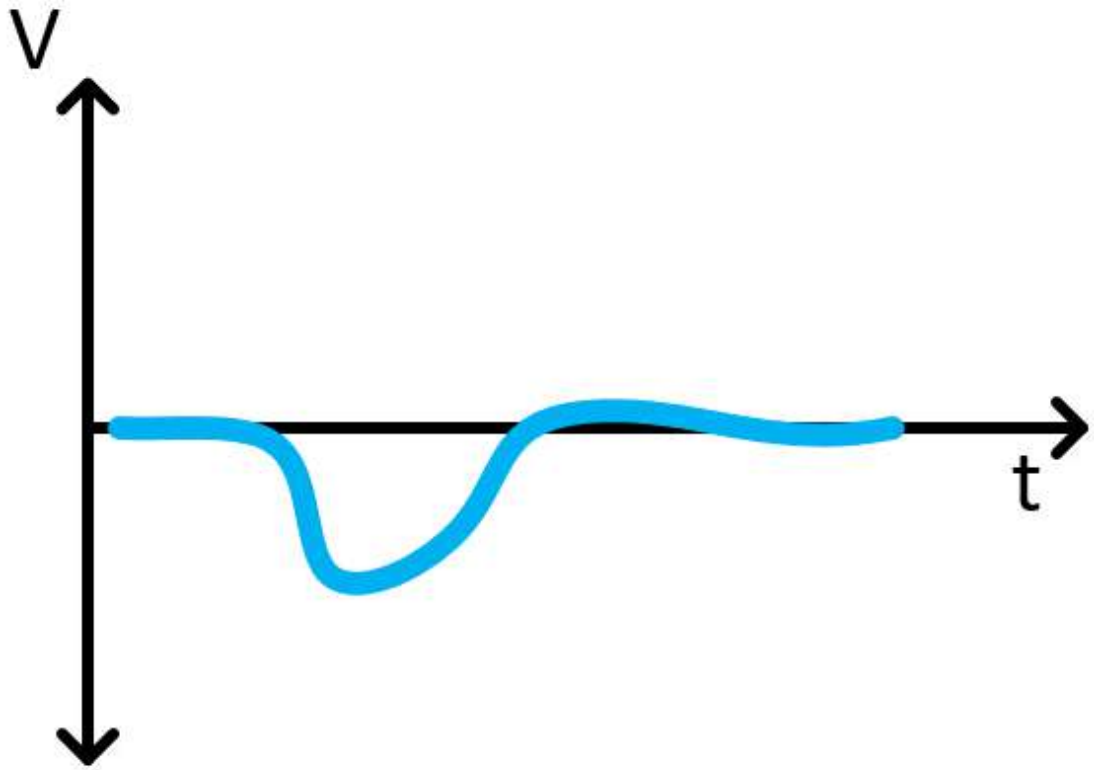
Input Filter Stability Simulation

No damping capacitor and bigger filter inductance value of **47uH/25mΩ(Rdc)**

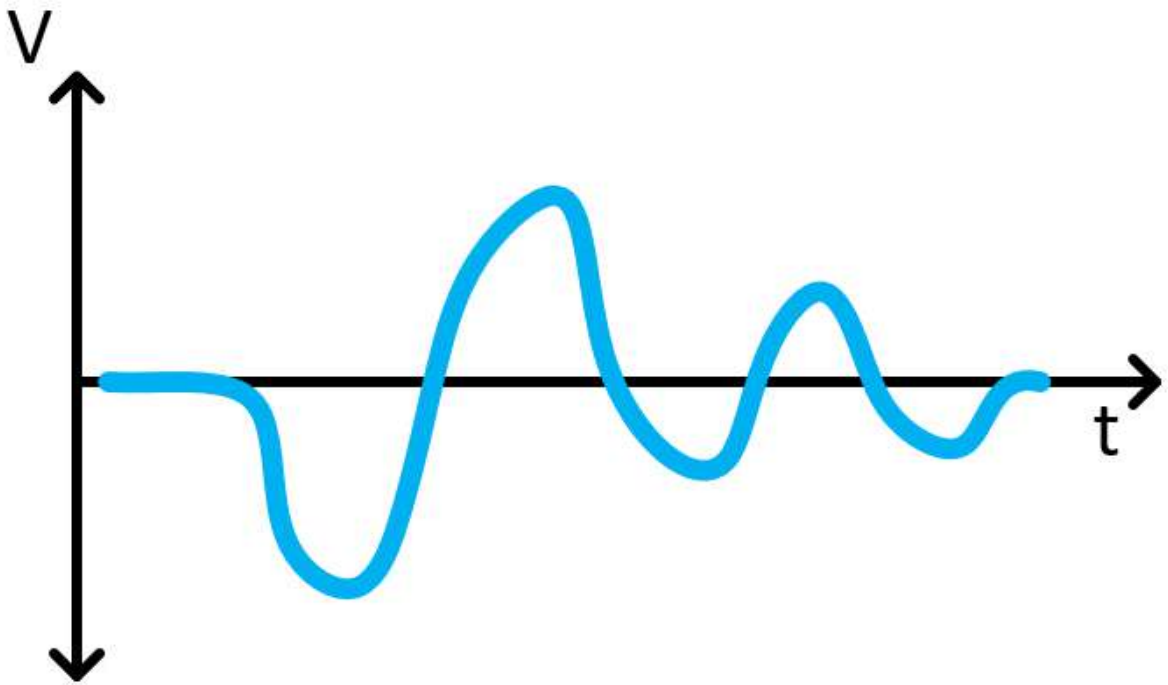


How to test DCDC Stability ?

Take a look at Vout and perform a max. load step during min. Vin



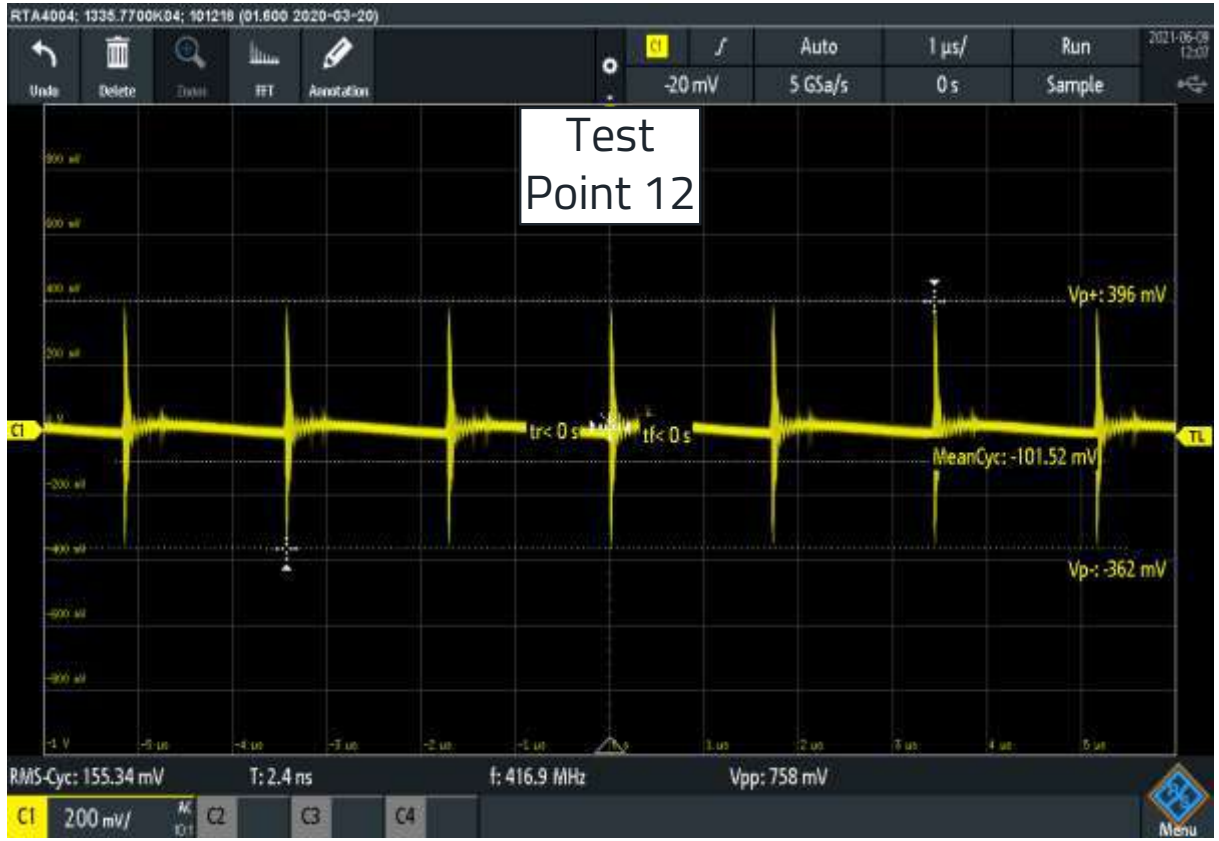
Stable Vout during load step



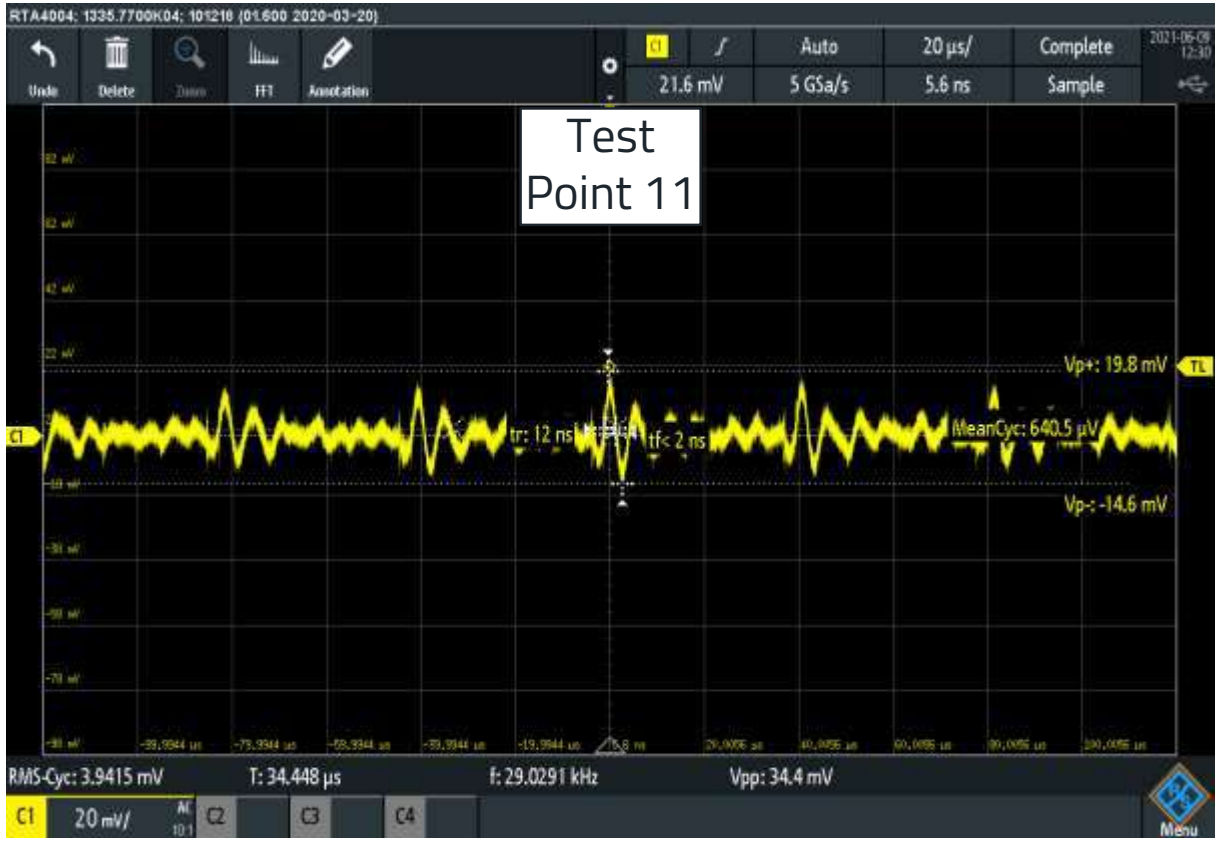
Unstable Vout during load step

Time Domain Measurements

PCB Test Points



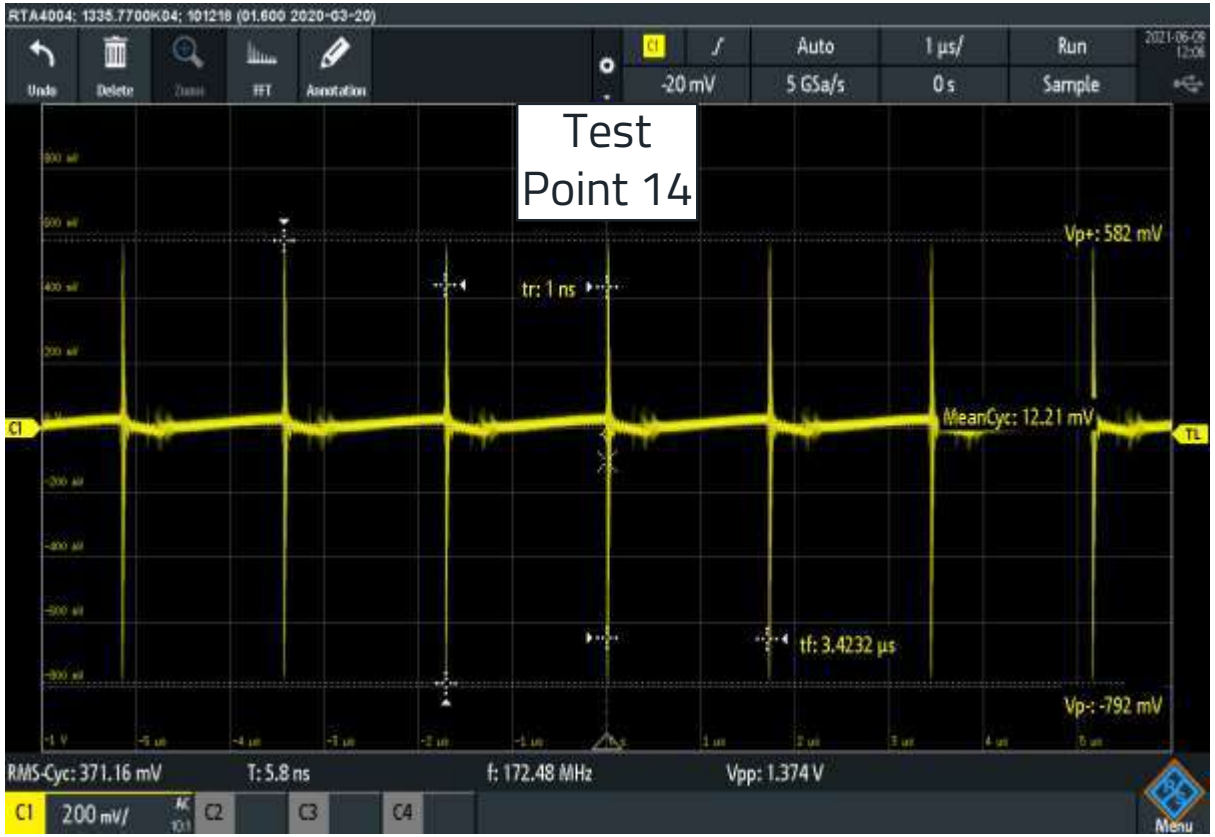
Bad Design Vin Ripple/Noise: 758mVpp



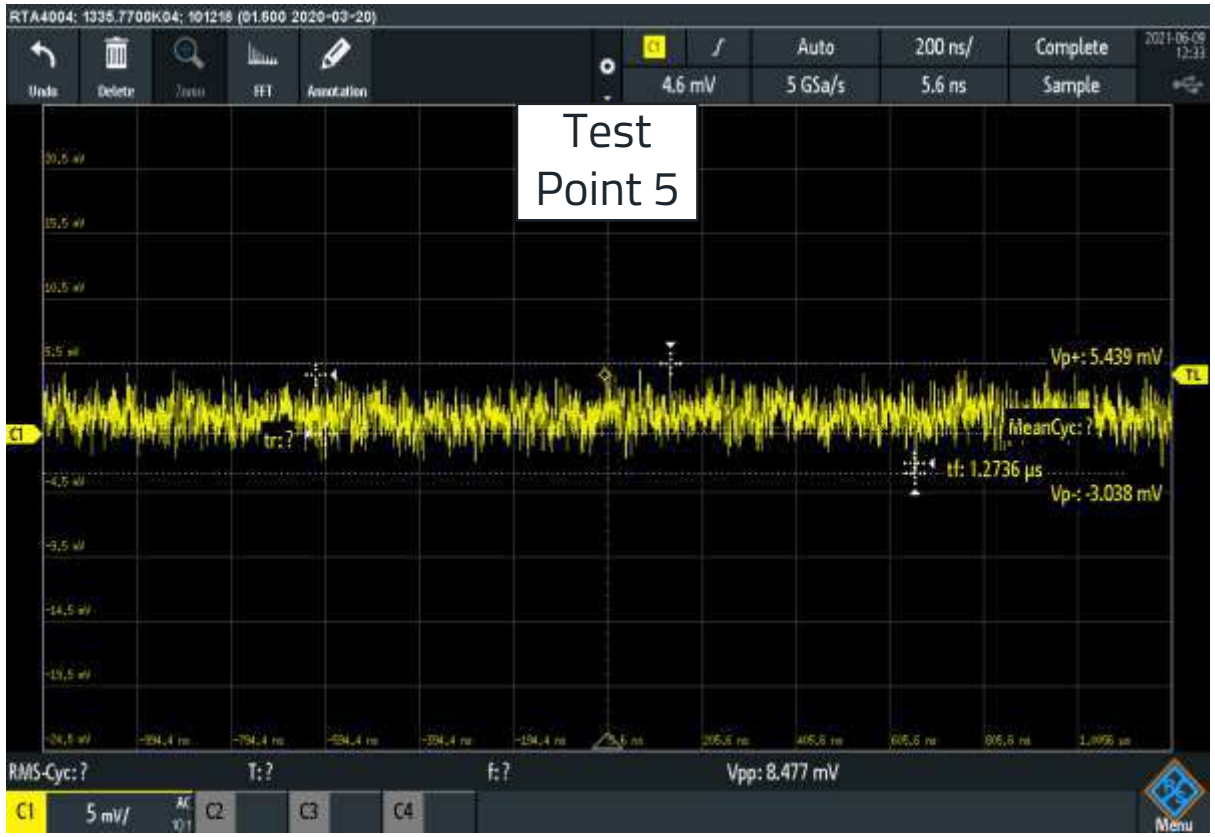
Good Design Vin Ripple/Noise: 34mVpp

Time Domain Measurements

PCB Test Points



Bad Design Vout Ripple/Noise: 1374mVpp

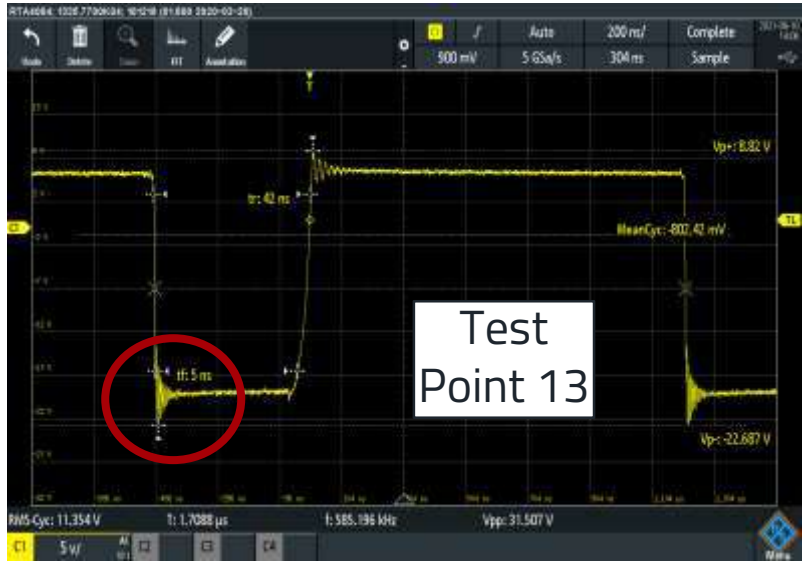


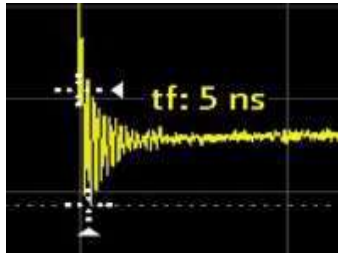
Good Design Vout Ripple/Noise: 8mVpp

Time Domain Measurements

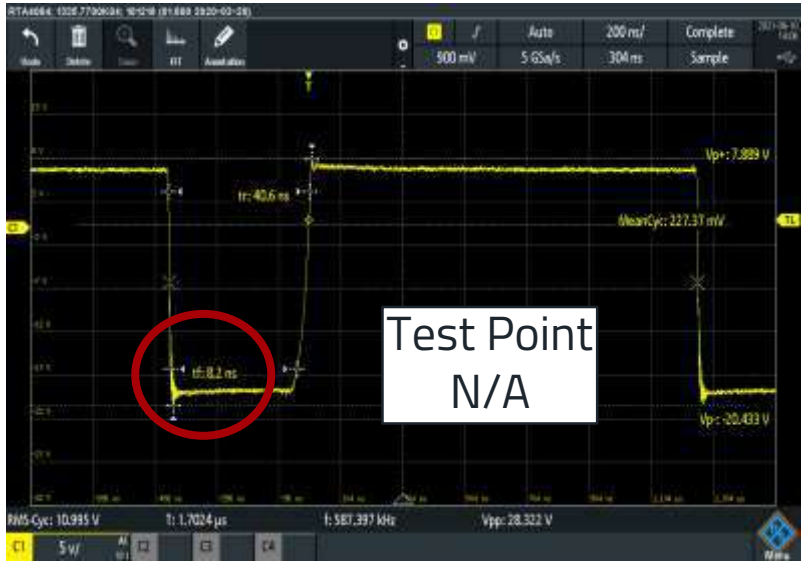
Switch Node Voltage

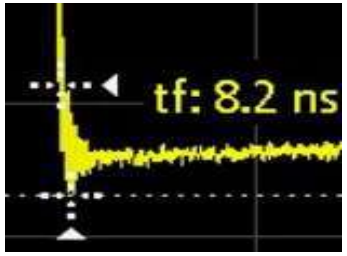
Bad Design



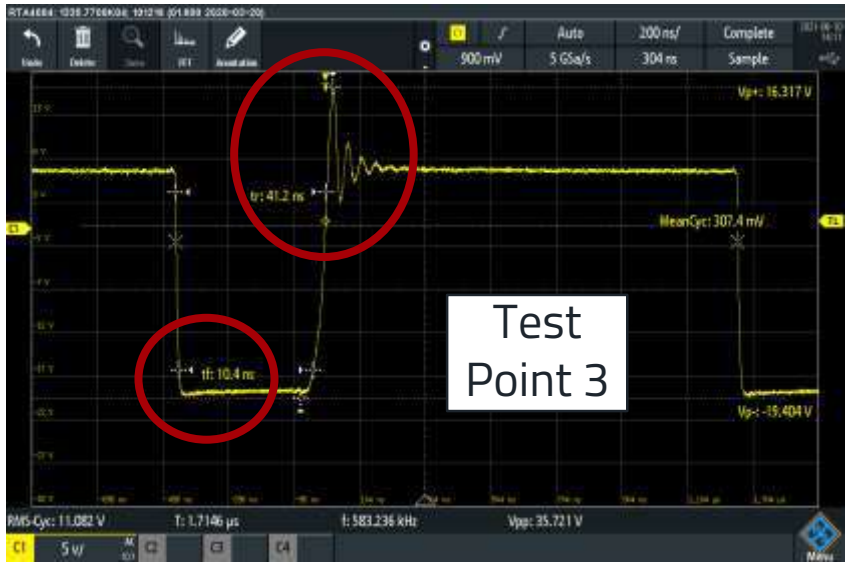


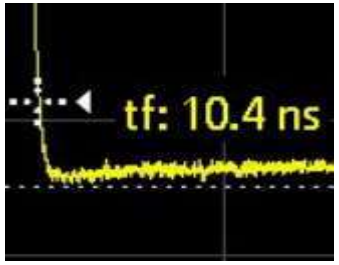
Good Design no Ferrite

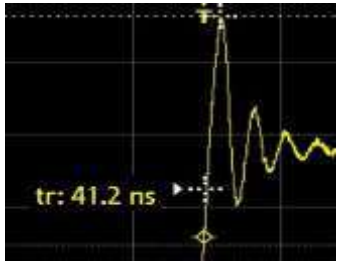




Good Design with Ferrite

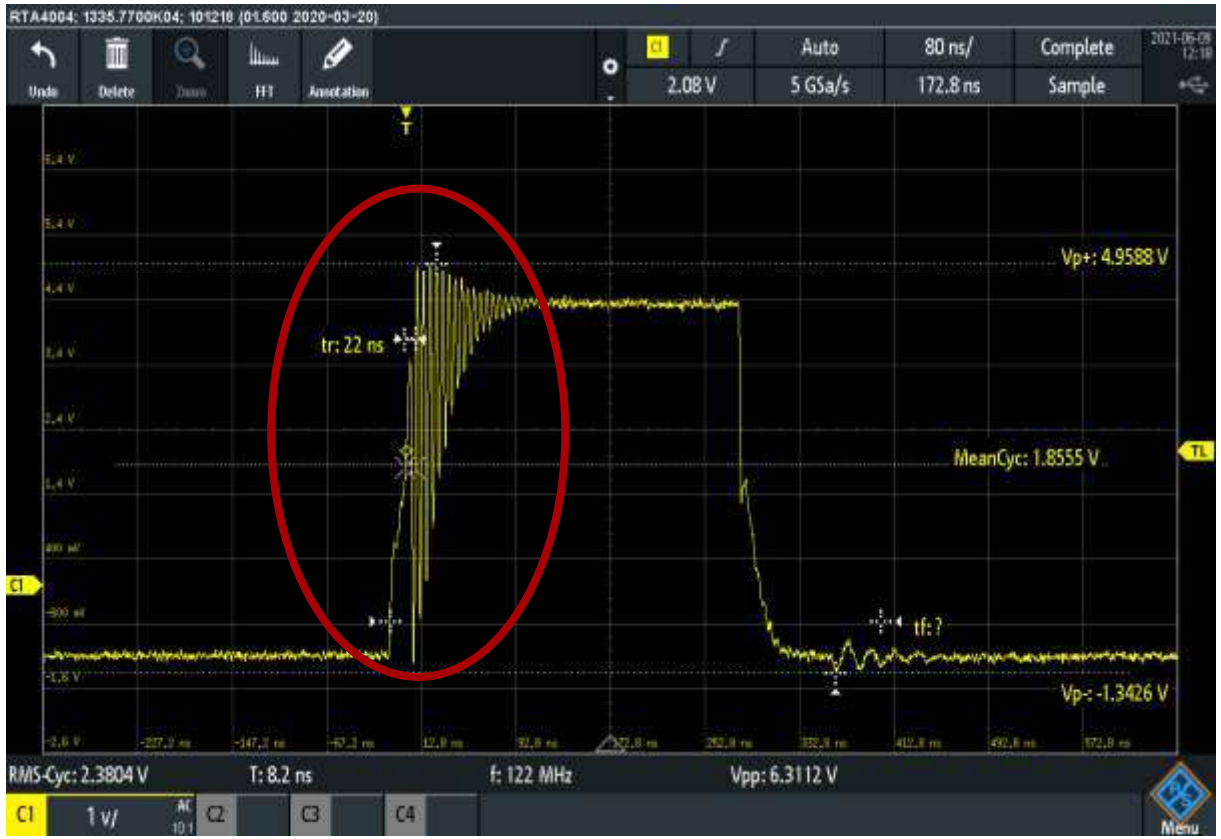






Time Domain Measurements

FET Gate Source Voltage

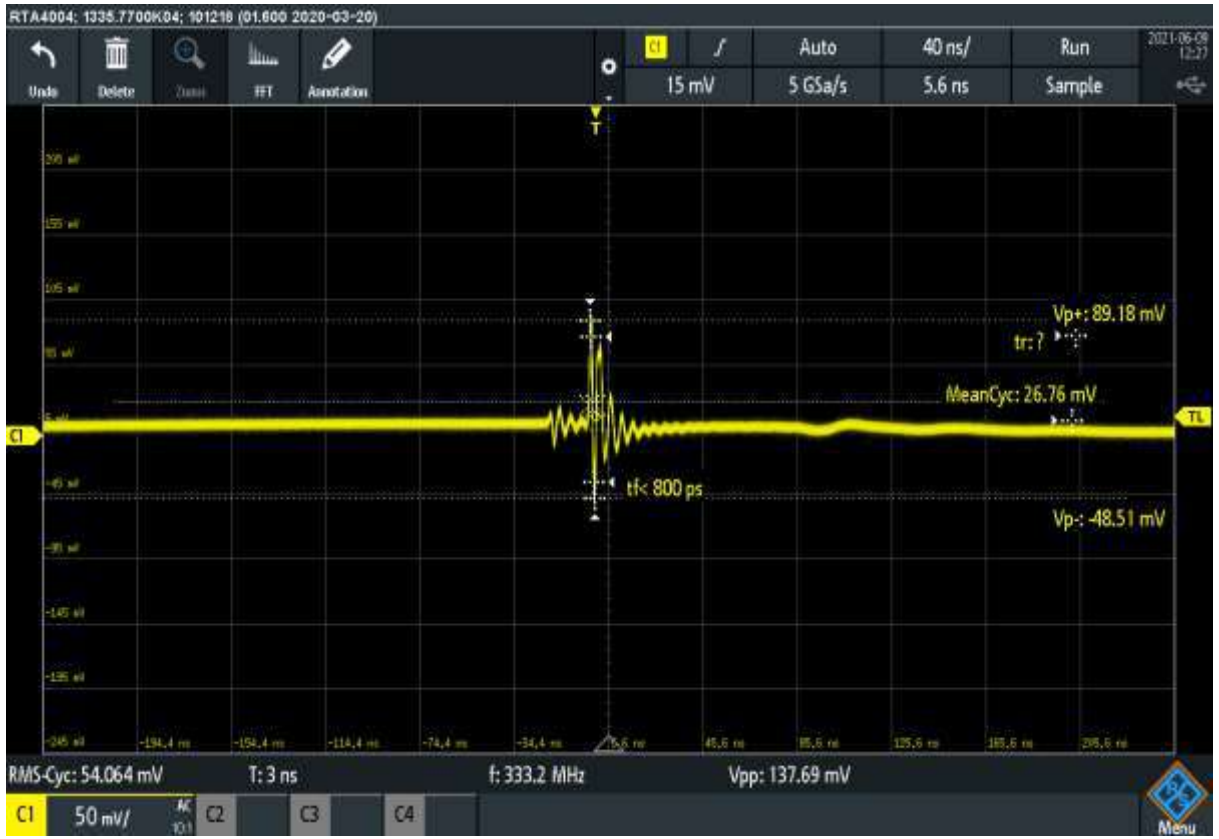


Bad Design Vgs MOSFET

Good Design Vgs MOSFET

Time Domain Measurements

Feedback PIN4 RF Voltage

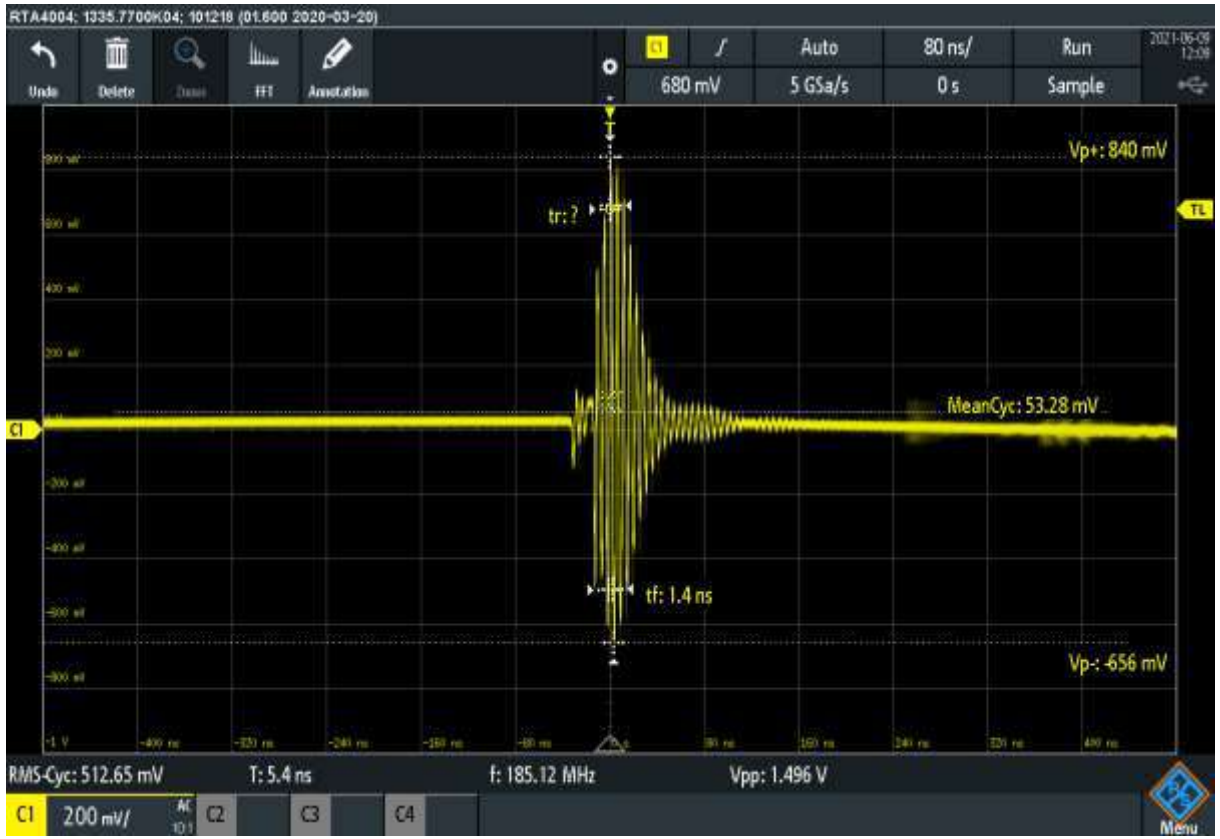


Bad Design Feedback Noise: 1078mVpp

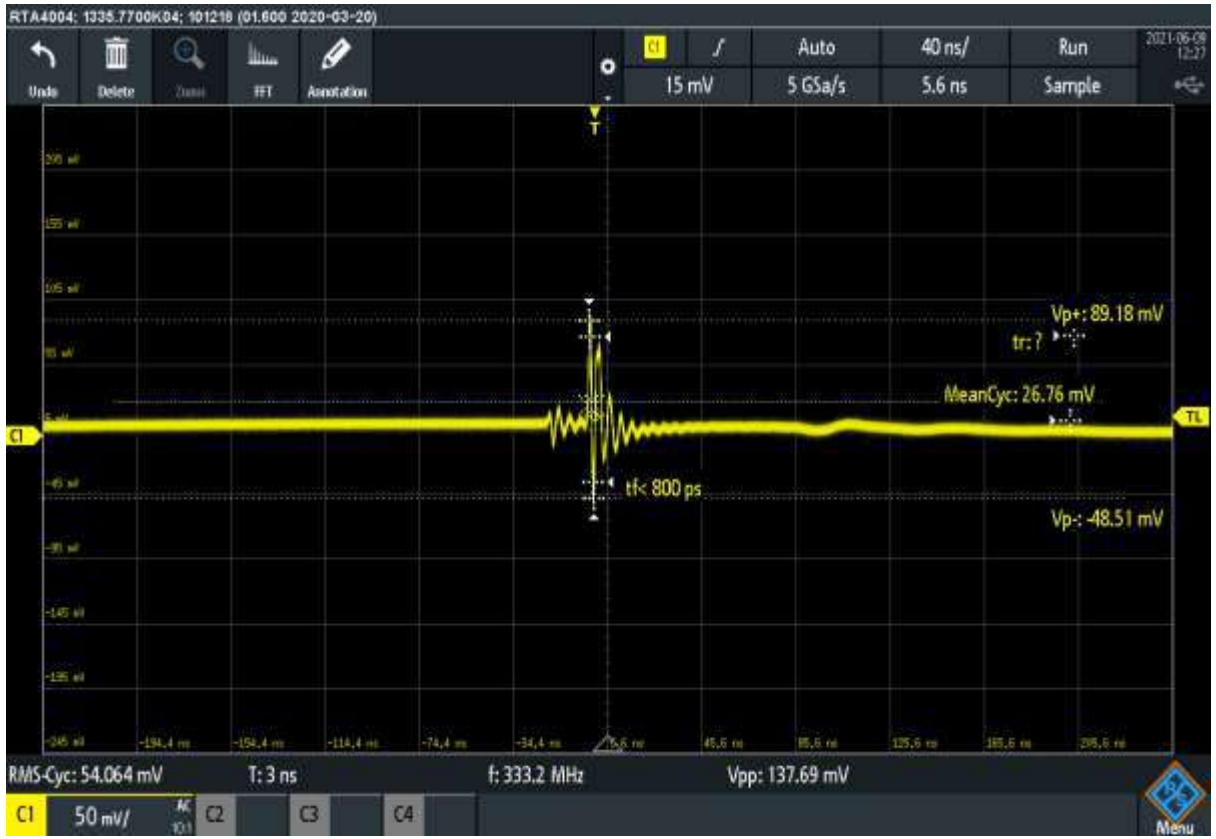
Good Design Feedback Noise: 137mVpp

Time Domain Measurements

Vcc PIN9 RF Voltage



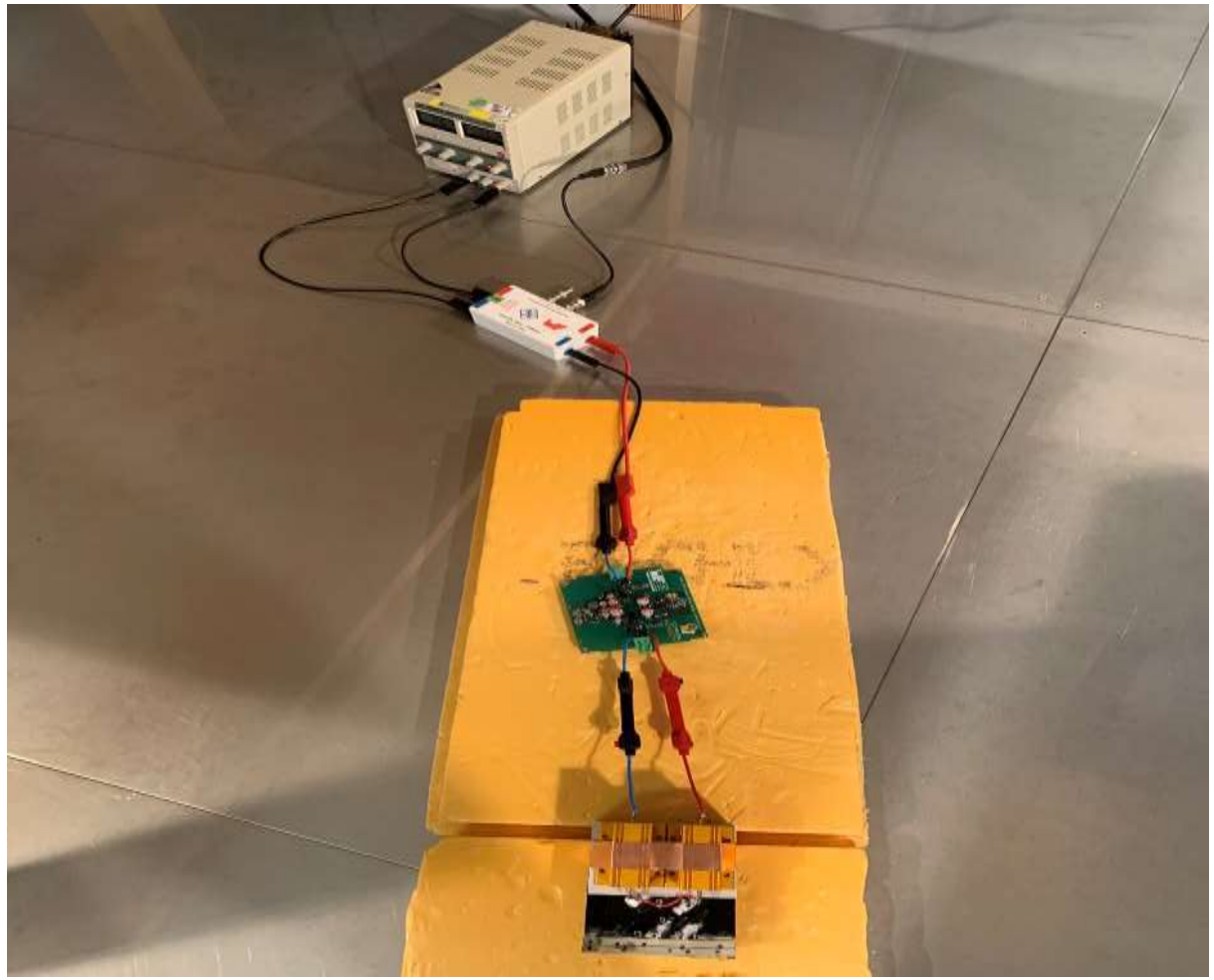
Bad Design I Vcc Pin Noise: 1496mVpp

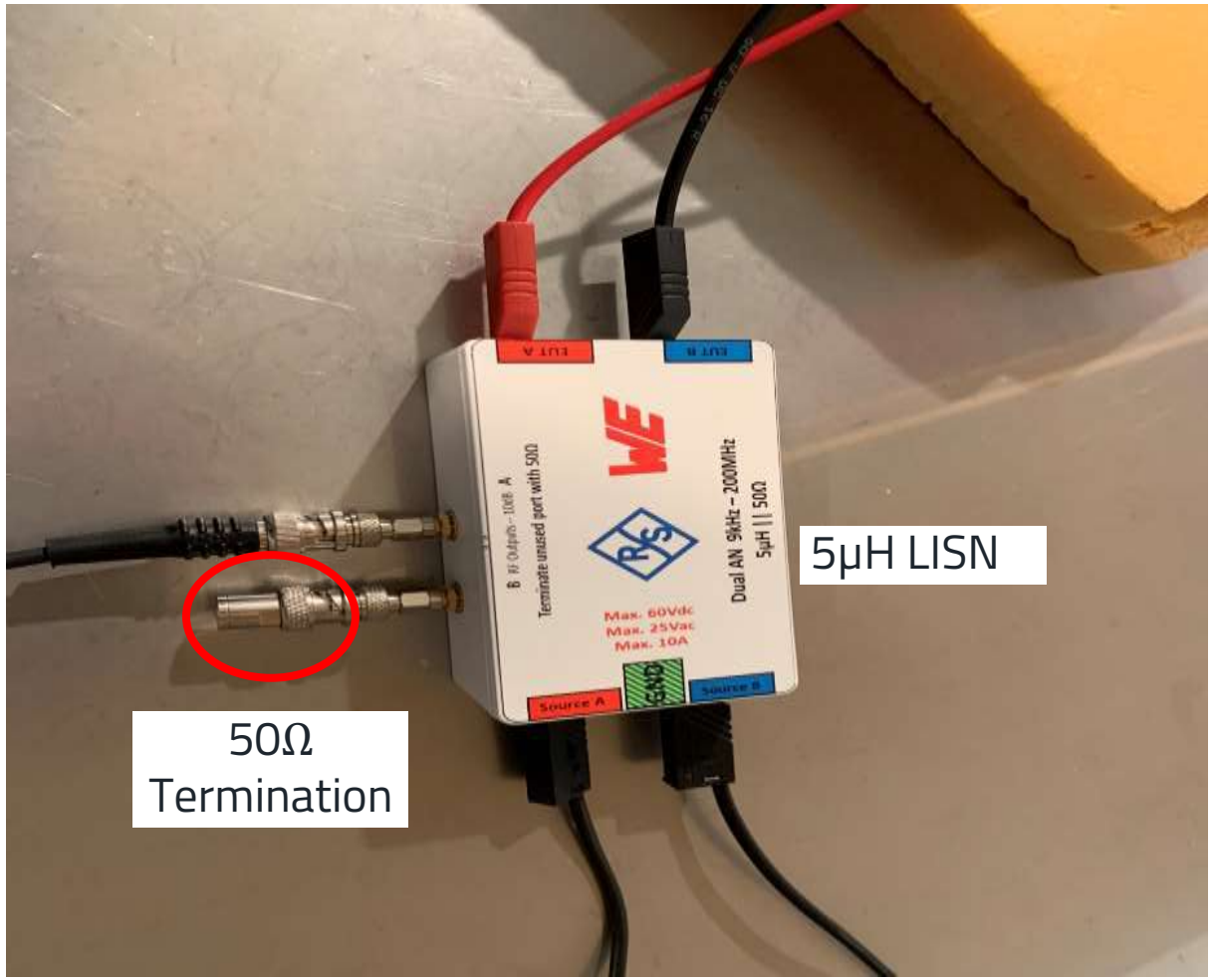


Good Design IC Vcc Pin Noise: 138mVpp

EMC Test Lab

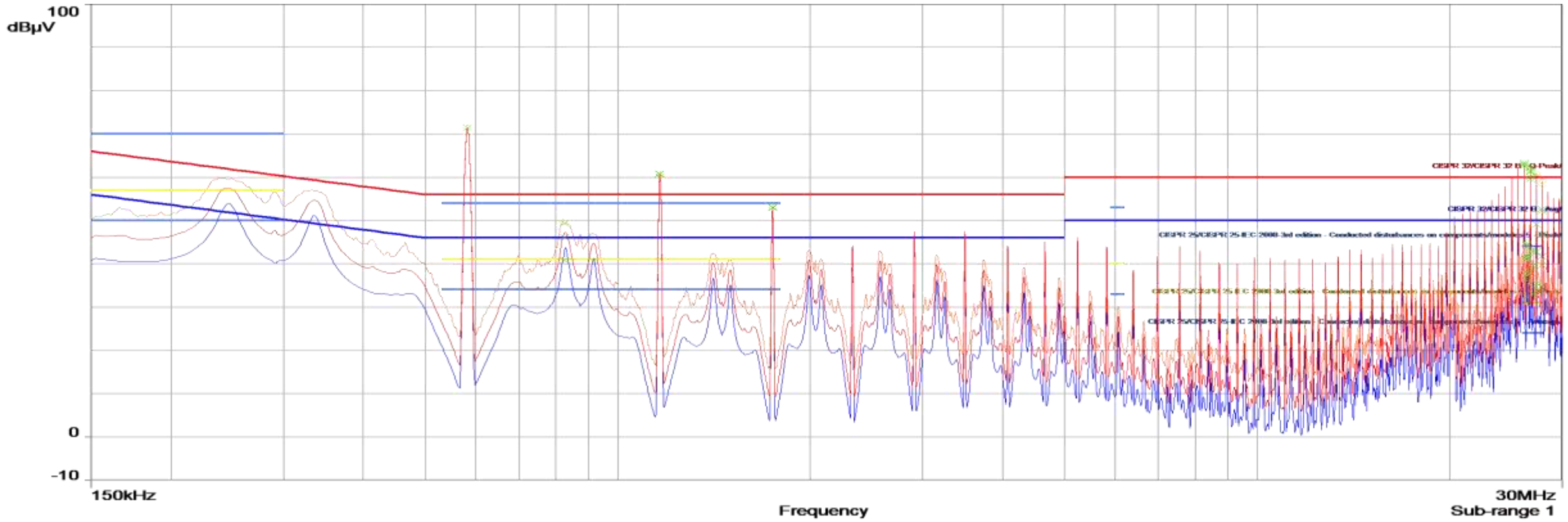
CISPR25 Conducted Emission





EMC Test Lab

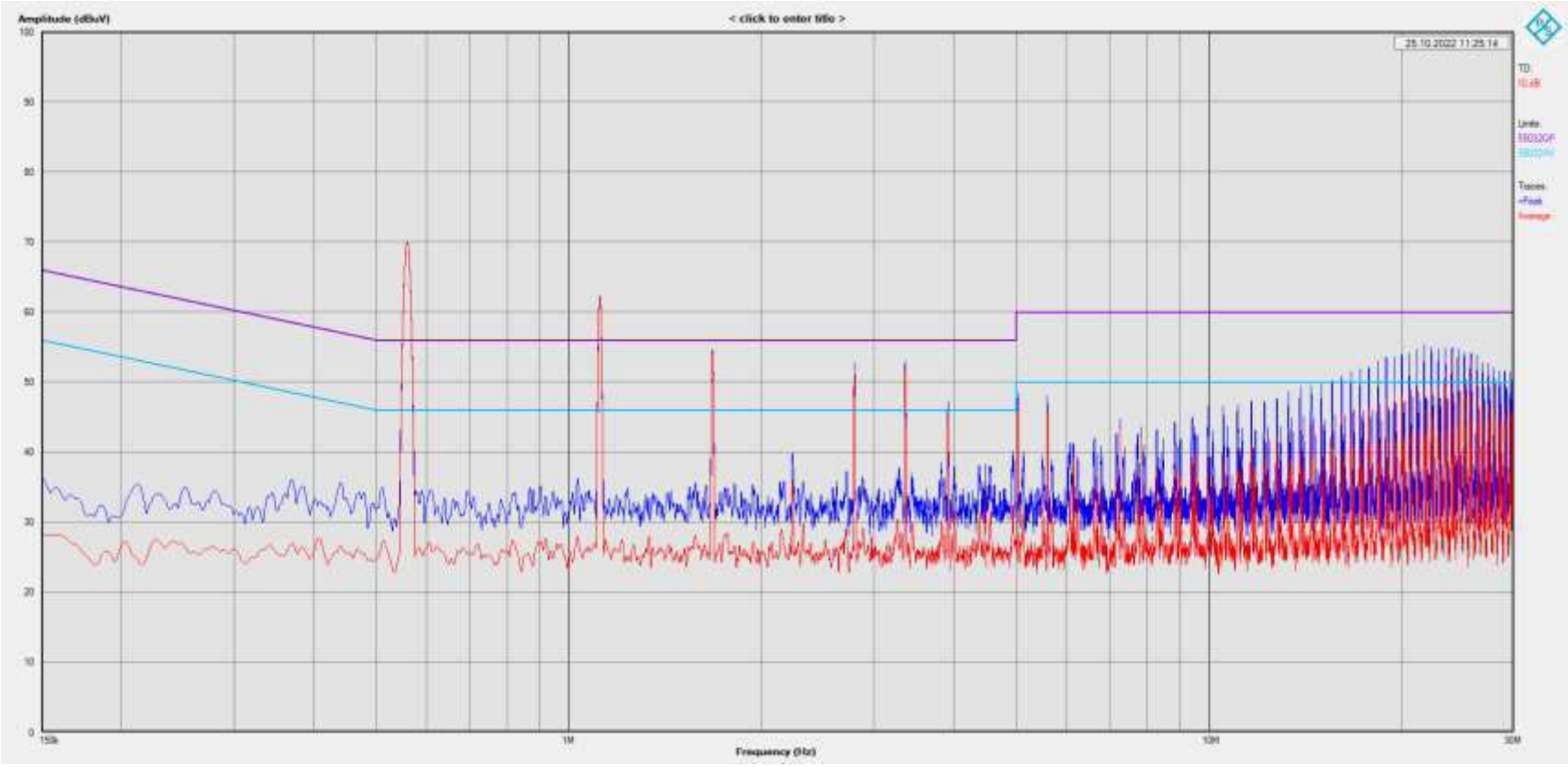
CISPR25 Conducted Emission



Bad Design; CISPR25 Class 5 and CISPR32 Class B Limit Lines

EMC Measurement

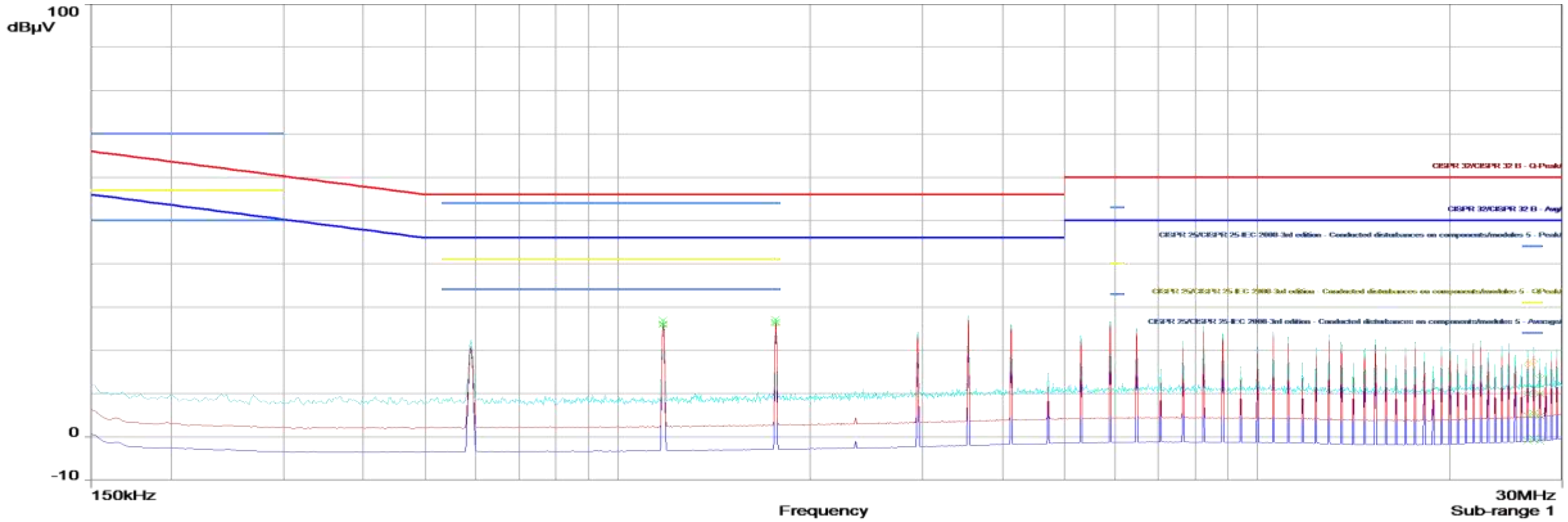
FAE Equipment Bad Design



Rohde & Schwarz EMI Debug Software + RTA4004

EMC Test Lab

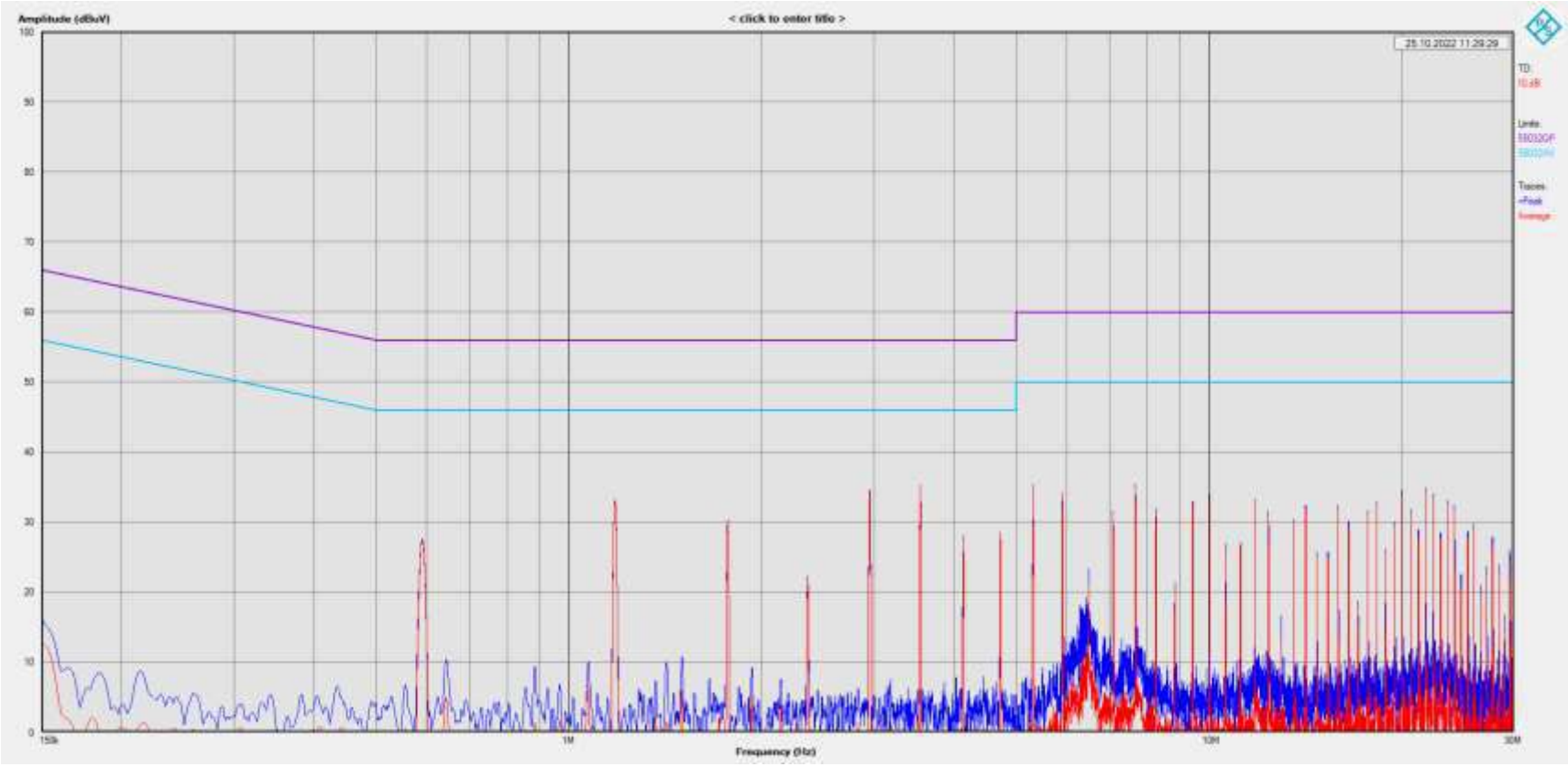
CISPR25 Conducted Emission



Good Design all Filter; CISPR25 Class 5 and CISPR32 Class B Limit Lines

EMC Measurement

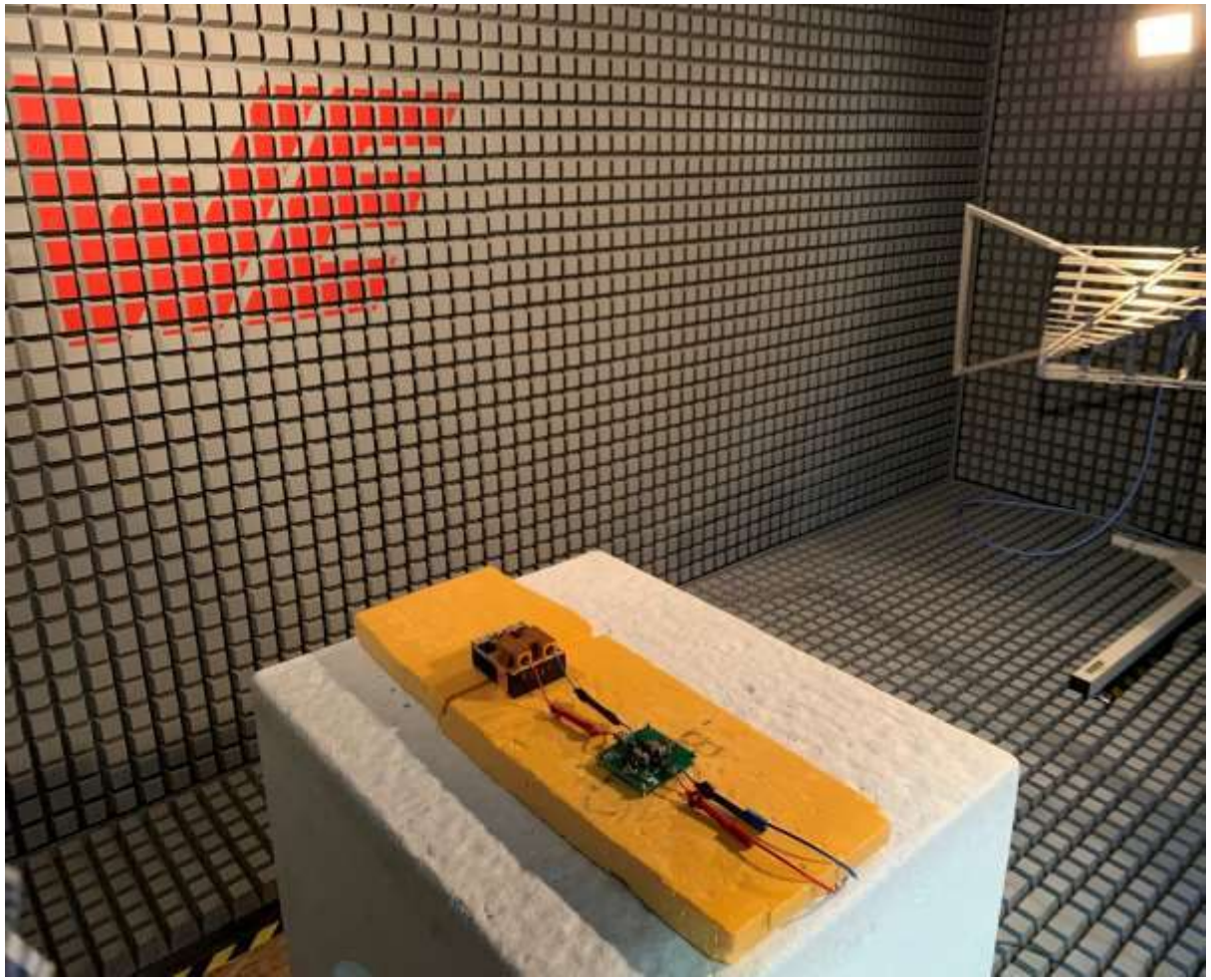
FAE Equipment Good Design

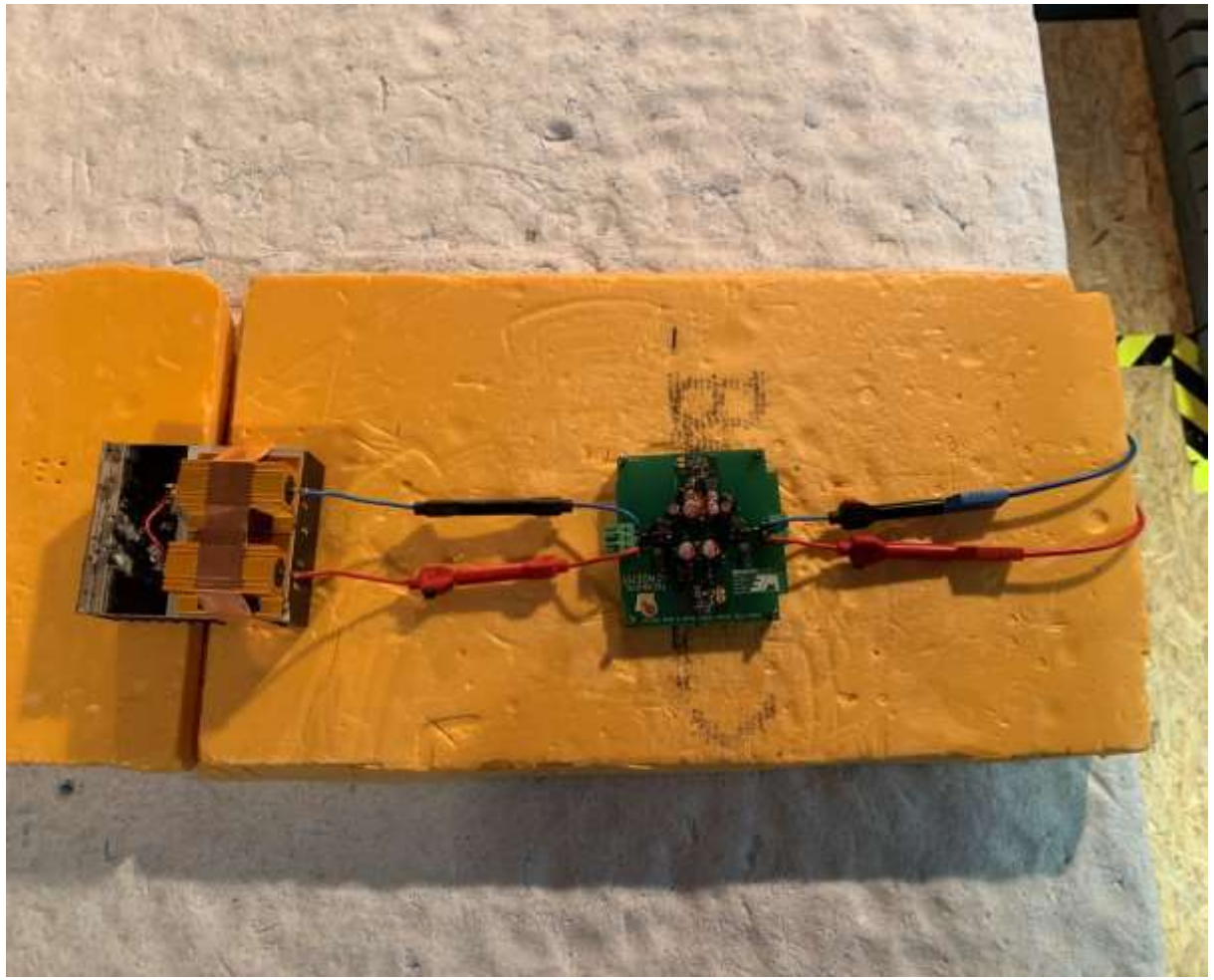


Rohde & Schwarz EMI Debug Software + RTA4004

EMC Test Lab

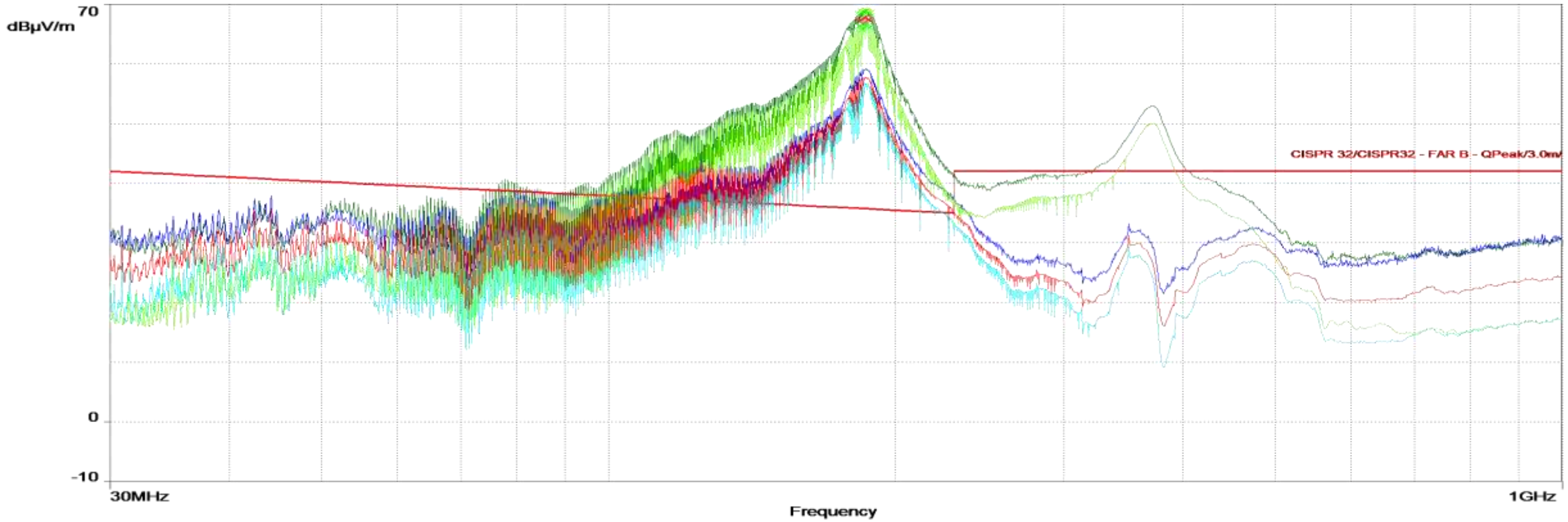
CISPR32 Radiated Emission





EMC Test Lab

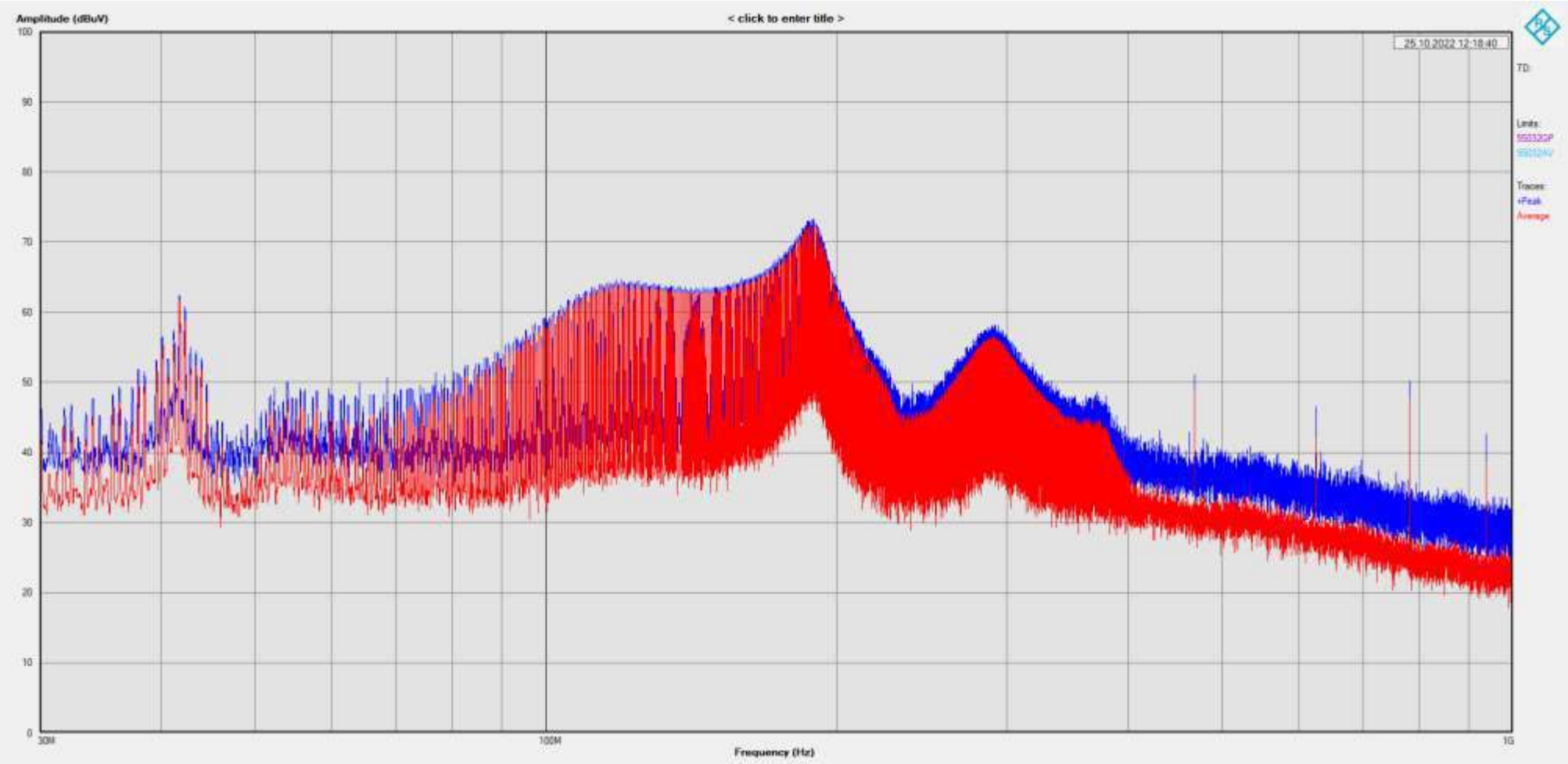
CISPR32 Radiated Emission



Bad Design

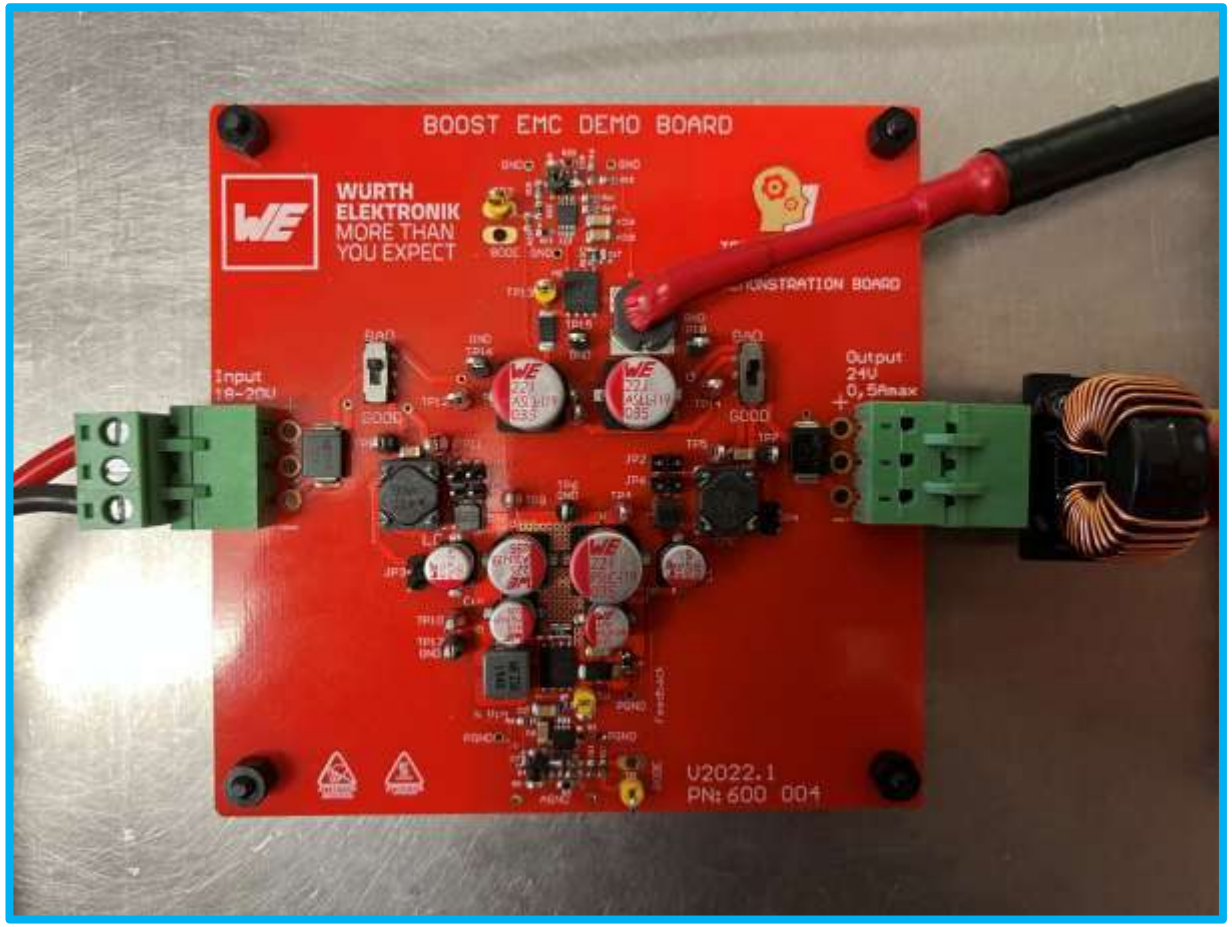
EMC Measurement Conducted 1GHz

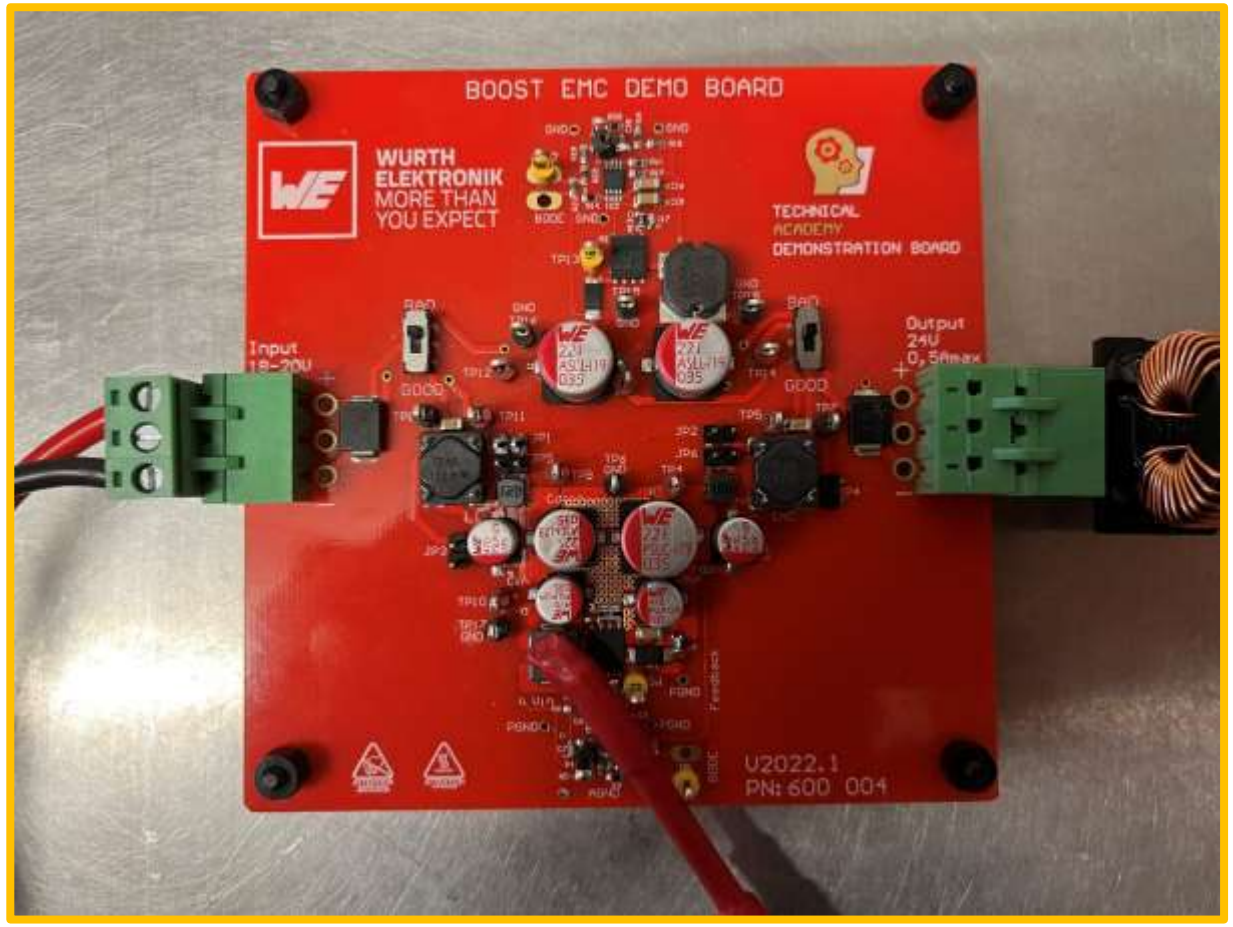
FAE Equipment Bad Design CM



Near Field 30MHz (H-Field Probe - Small Loop – Power Inductor)

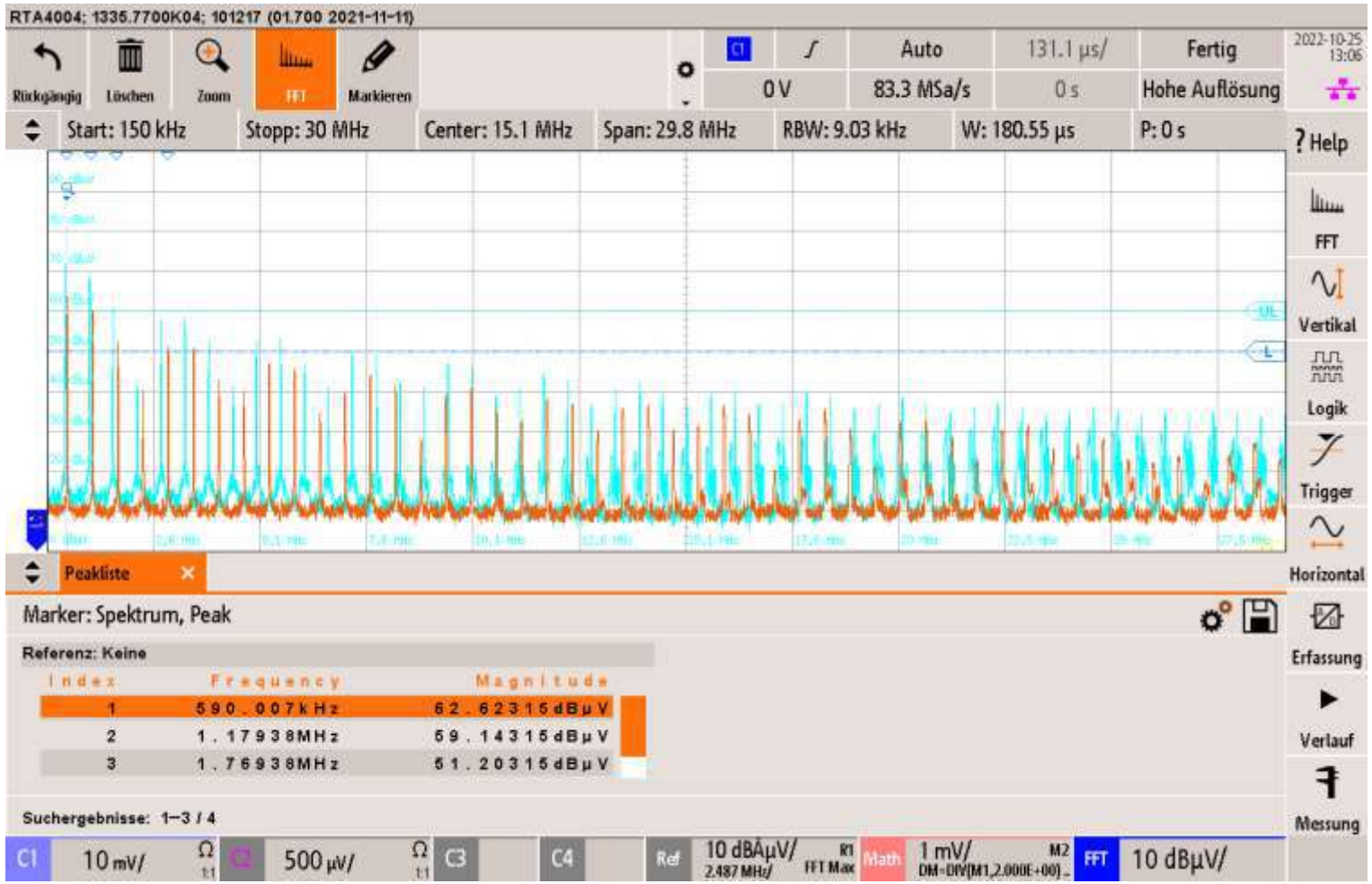
Bad vs. Good





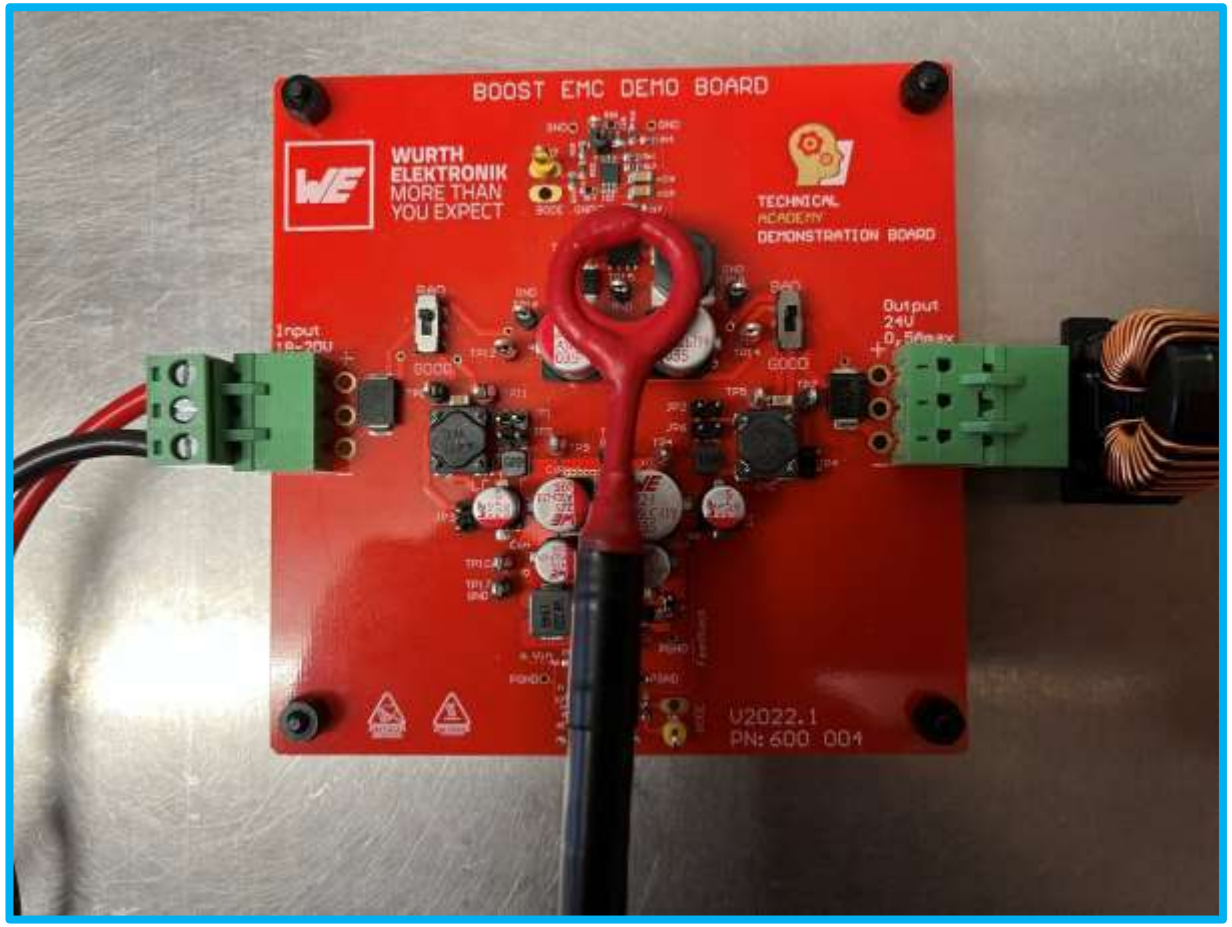
Near Field 30MHz (H-Field Probe - Small Loop – Power Inductor)

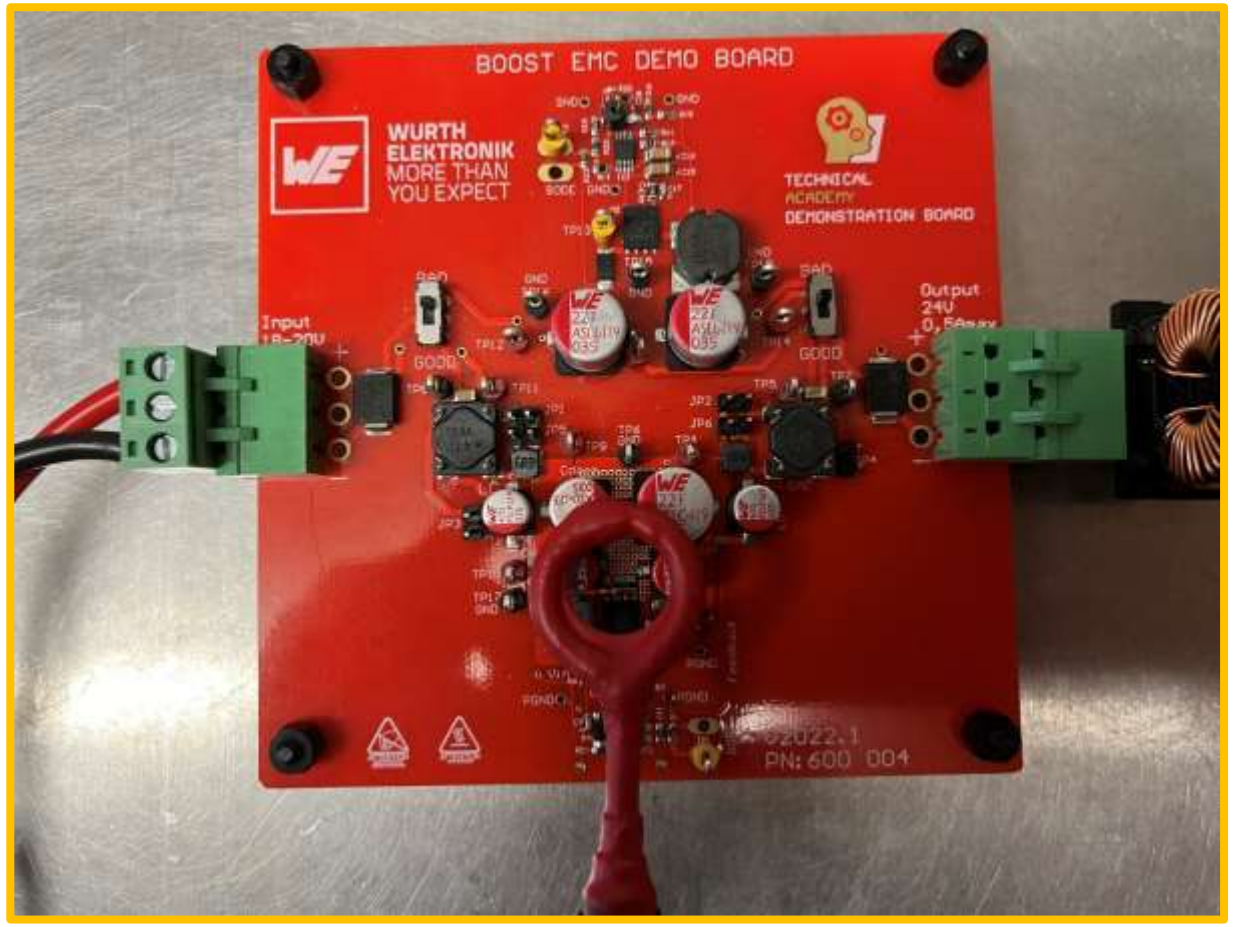
Bad vs. Good



Near Field 1GHz (H-Field Probe - Big Loop)

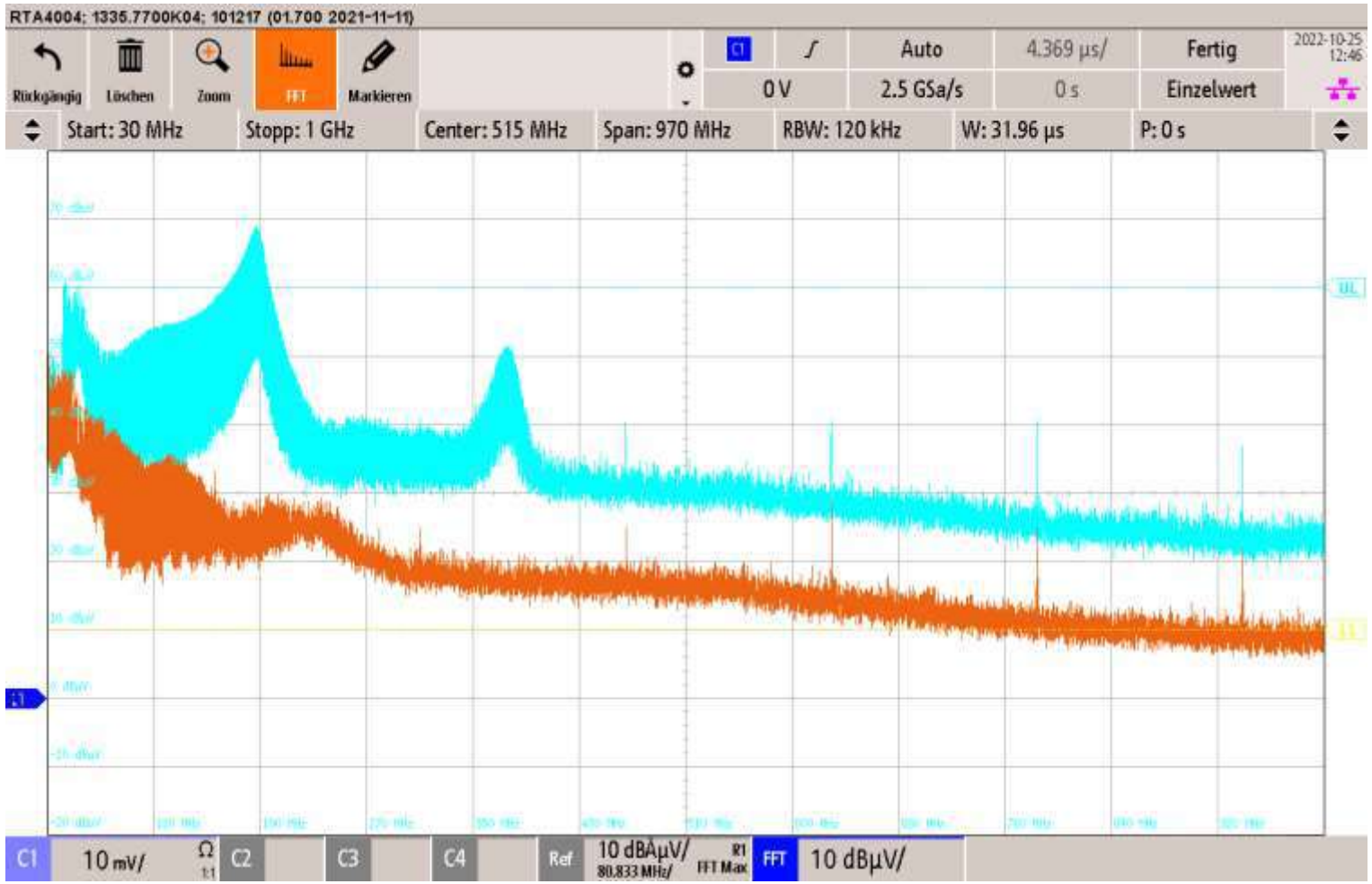
Bad vs. Good





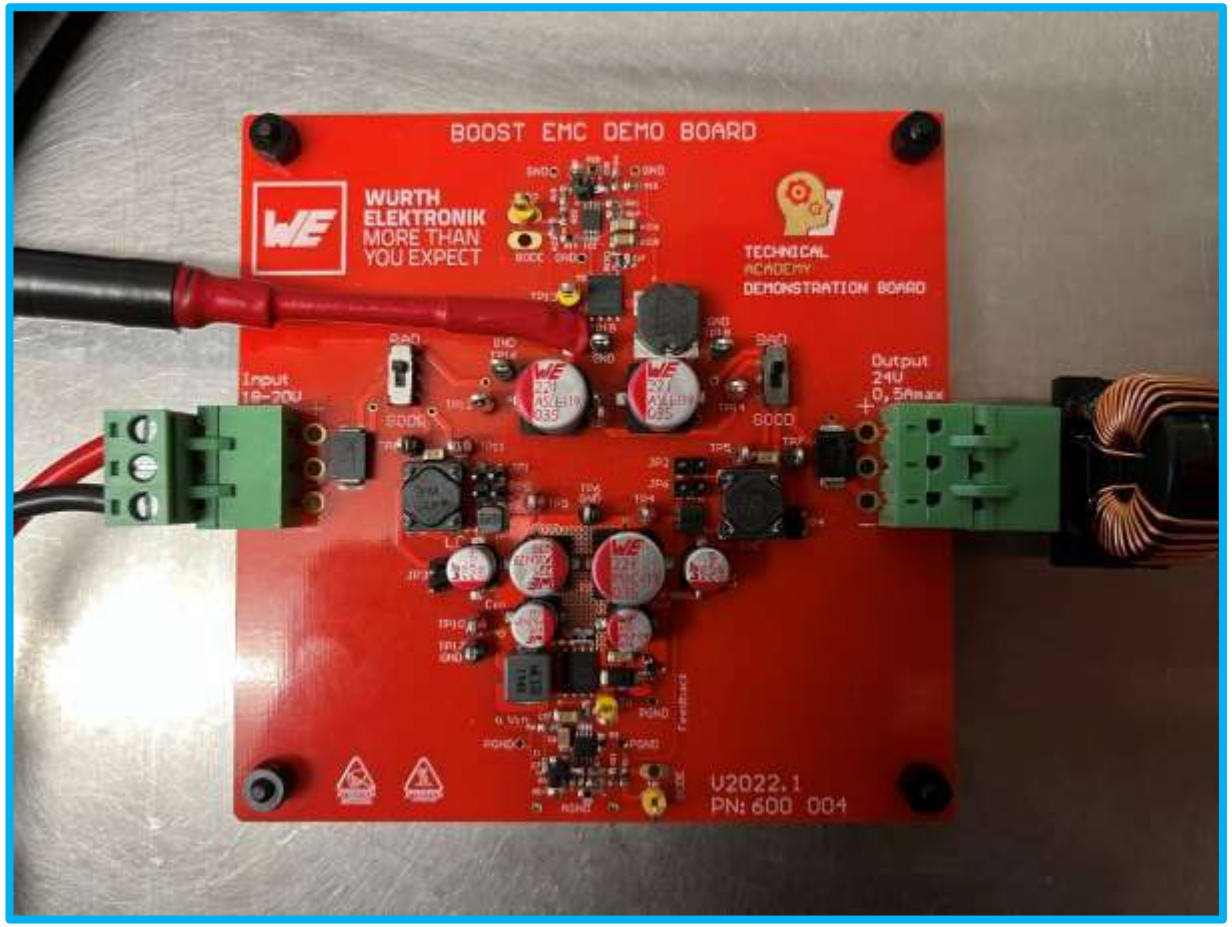
Near Field 1GHz (H-Field Probe - Big Loop)

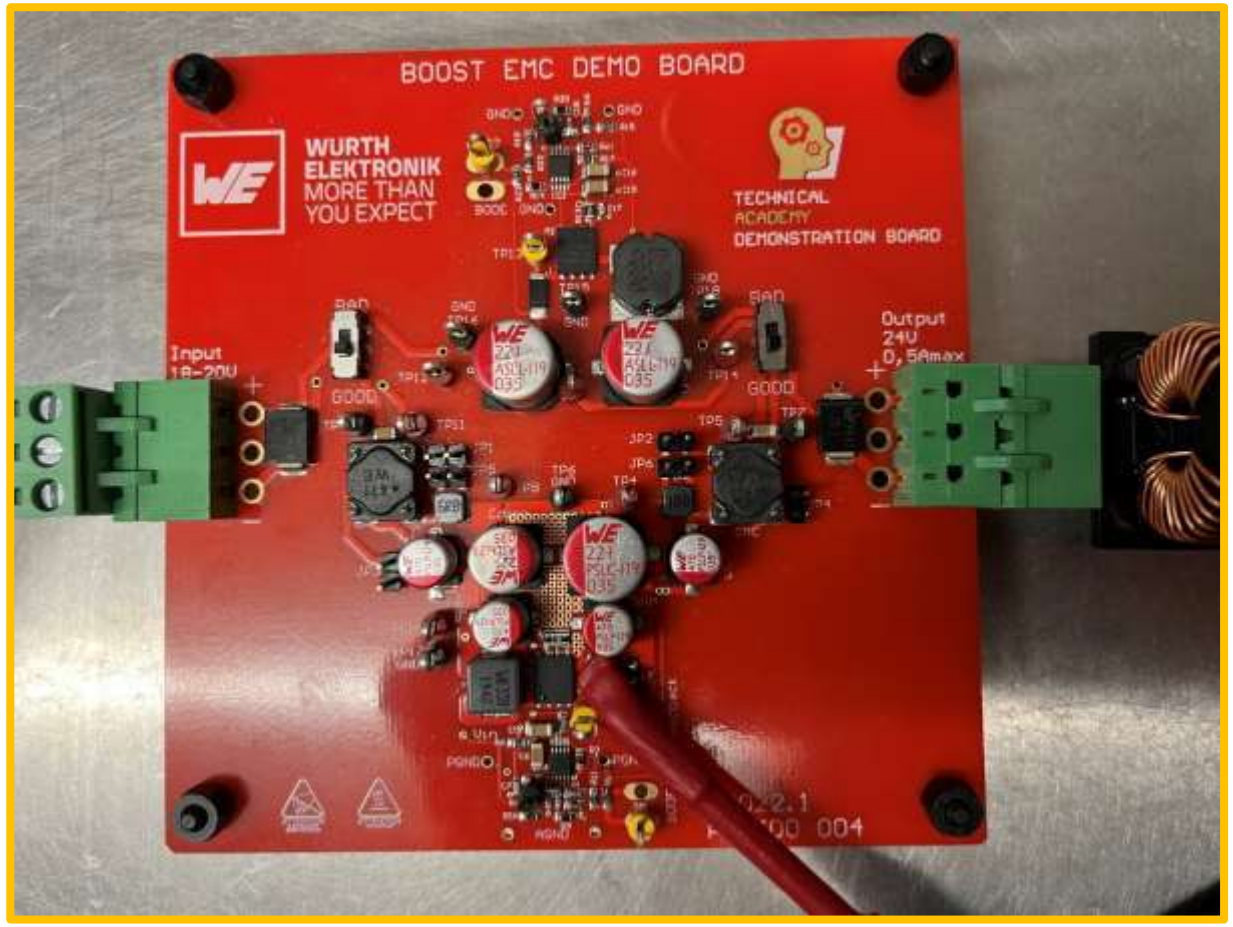
Bad vs. Good



Near Field 1GHz (H-Field Probe - Small Loop - Schottky Diode)

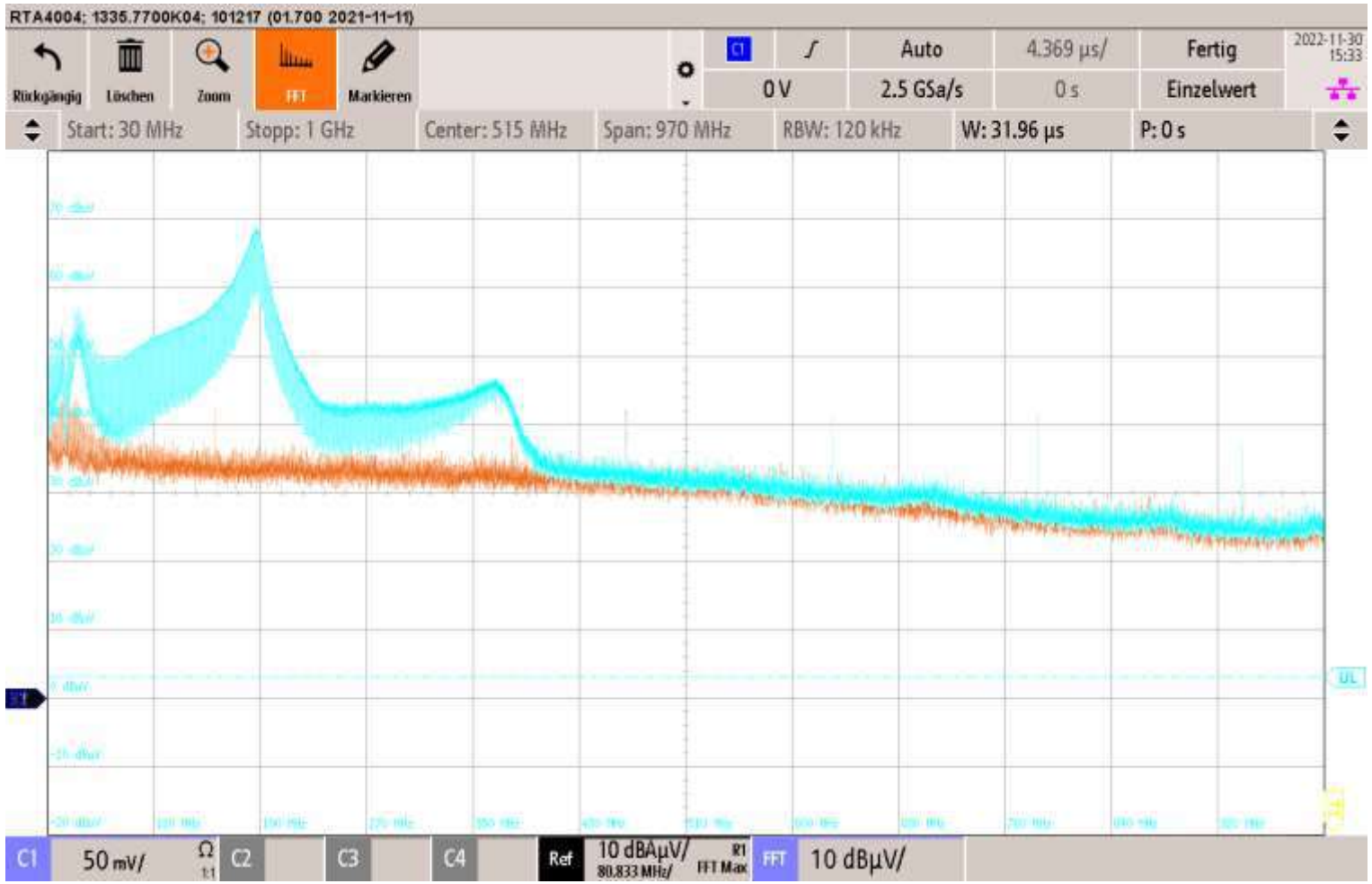
Bad vs. Good





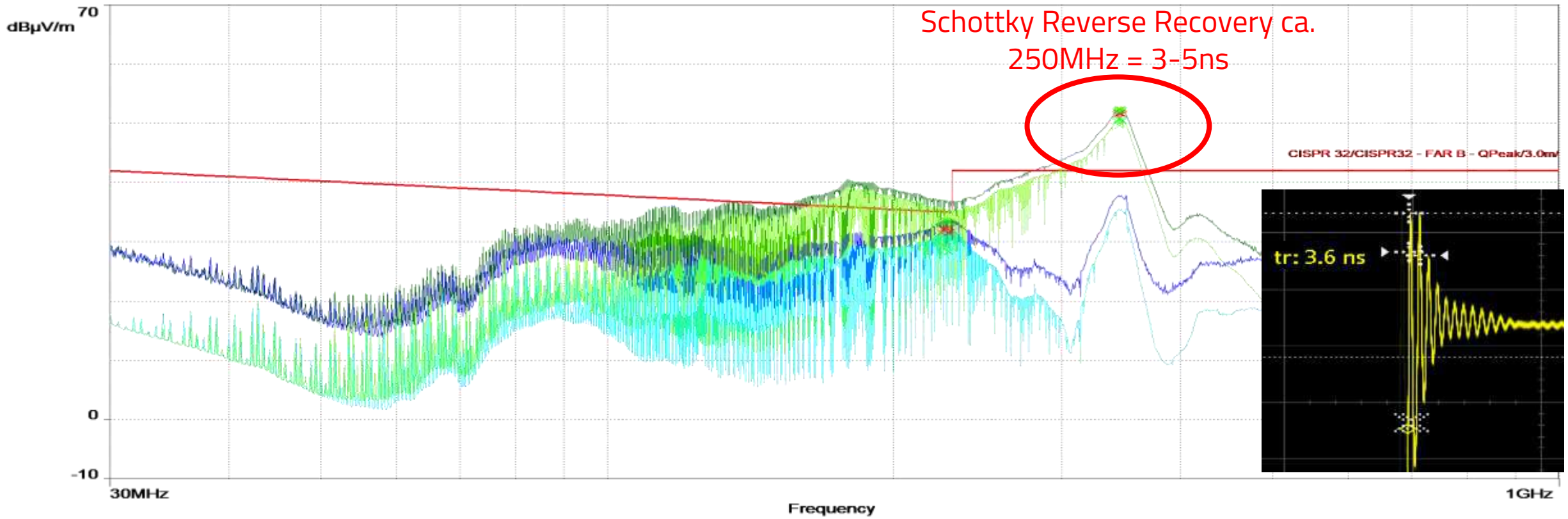
Near Field 1GHz (H-Field Probe - Small Loop - Schottky Diode)

Bad vs. Good



EMC Test Lab

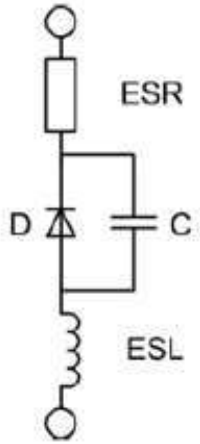
CISPR32 Radiated Emission

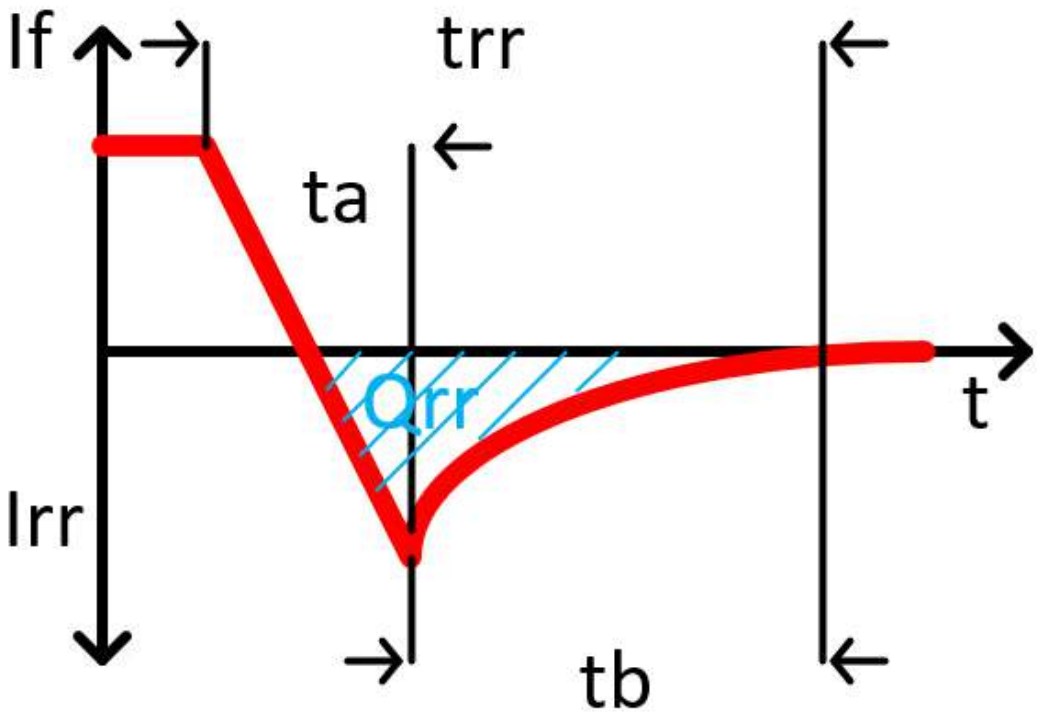


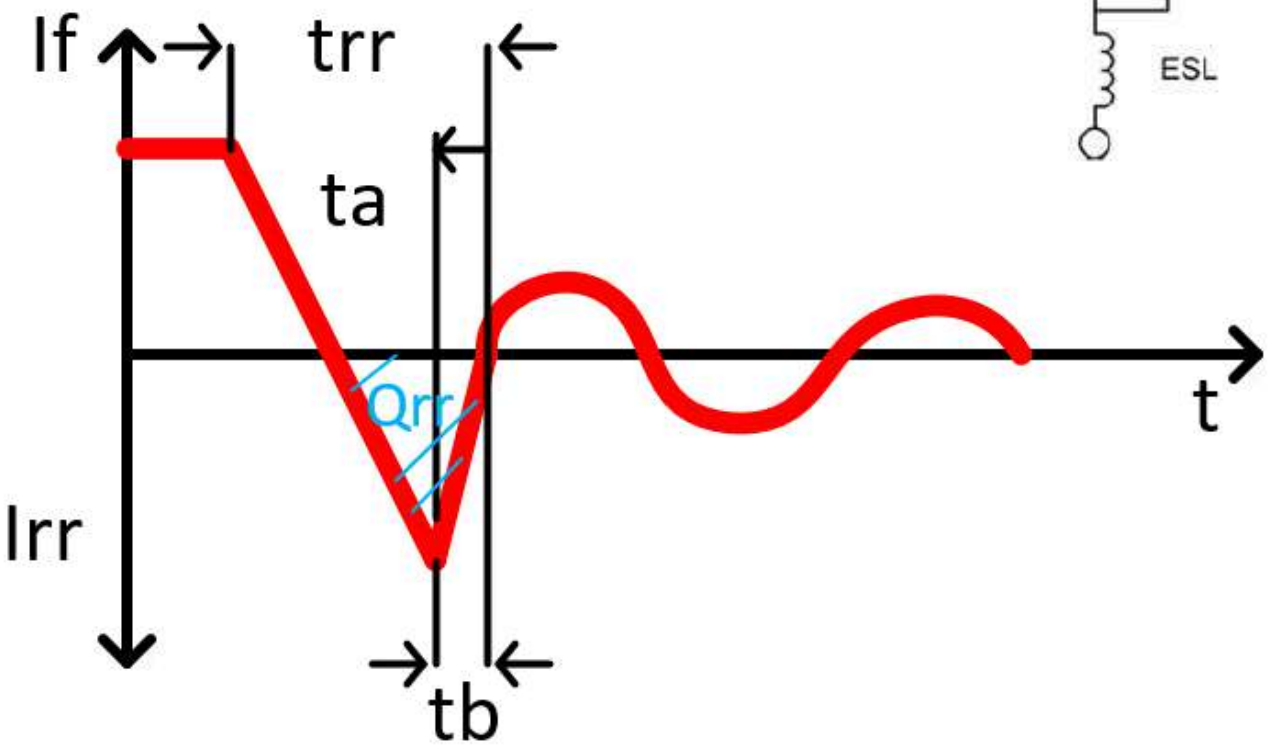
Good Design: No Filters and no Chip Bead Ferrite after Schottky Diode

Schottky Diode Reverse Recovery Current

Recovery time „tb“ is critical due to possible oscillations







The softer the recovery, the lower the RF EMI noise but the higher the losses „Qrr“ in the diode

Redexpert

Chip Bead Selection @ 0,5A Iout and 250MHz → Reactance XL under 10MHz as low as possible!

REDEXPERT | FERRITES FOR PCB ASSEMBLY | APPLICATIONS | HOW TO | SHARE | 4 ITEMS | ANDREAS

Filters: Size = 0805

Order Code	Series	Size	I...	Spec	Type	Z@100MHz	Z_{max}	$Z_{0.50\,A}$@250 MHz	$R_{0.50\,A}$@250 MHz	R_{DC}	I_R	L	W	H	Pin L...	Lines	Assembli...	
742792037	WE-CBF	0805			High Current	330 Ω	375 Ω @250 MHz	164 Ω	92.6 Ω	80.0 mΩ	2.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792038	WE-CBF	0805			Wide Band	240 Ω	280 Ω @250 MHz			400 mΩ	1.40 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792040	WE-CBF	0805			High Current	600 Ω	700 Ω @150 MHz	240 Ω	130 Ω	150 mΩ	2.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
74279205	WE-CBF	0805			Wide Band	1.00 kΩ	1.05 kΩ @120 MHz			450 mΩ	900 mA	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
74279206	WE-CBF	0805			High Current	30.0 Ω	55.0 Ω @1.00 GHz	30.5 Ω	24.2 Ω	25.0 mΩ	3.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792063	WE-CBF	0805			High Current	60.0 Ω	90.0 Ω @500 MHz	43.4 Ω	34.8 Ω	25.0 mΩ	3.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792064	WE-CBF	0805			High Speed	75.0 Ω	300 Ω @500 MHz			200 mΩ	1.70 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
74279207	WE-CBF	0805			High Current	100 Ω	140 Ω @400 MHz	56.6 Ω	35.1 Ω	150 mΩ	1.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1

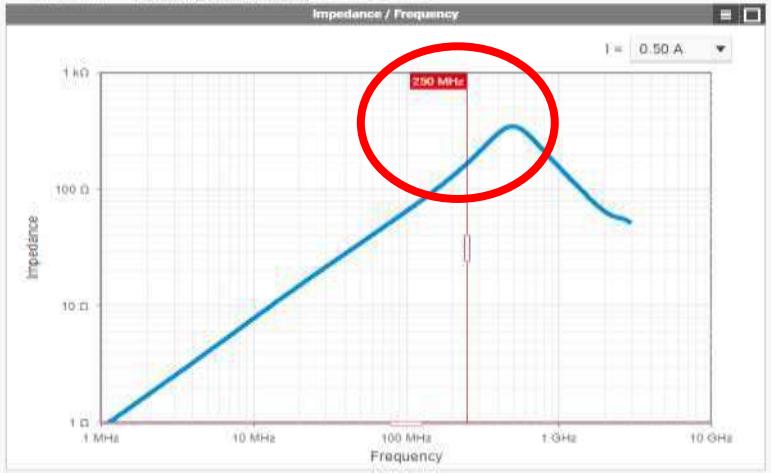
System | Pulse | LOG OUT | DOWNLOAD MODULES | ADD | MORE

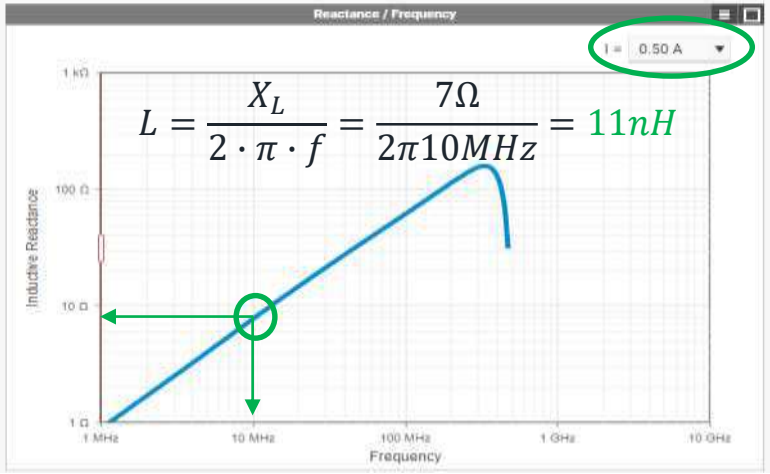
742792037 WE-CBF · 0805 330 Ω

Click and type or drop an Order Code here

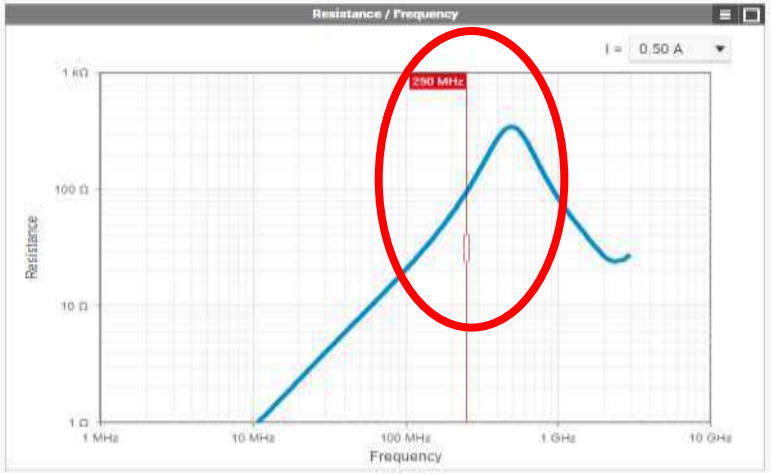
Z = 164Ω / R = 93 Ω @ 250MHz

Show Panel: Z vs. F | X vs. F | R vs. F



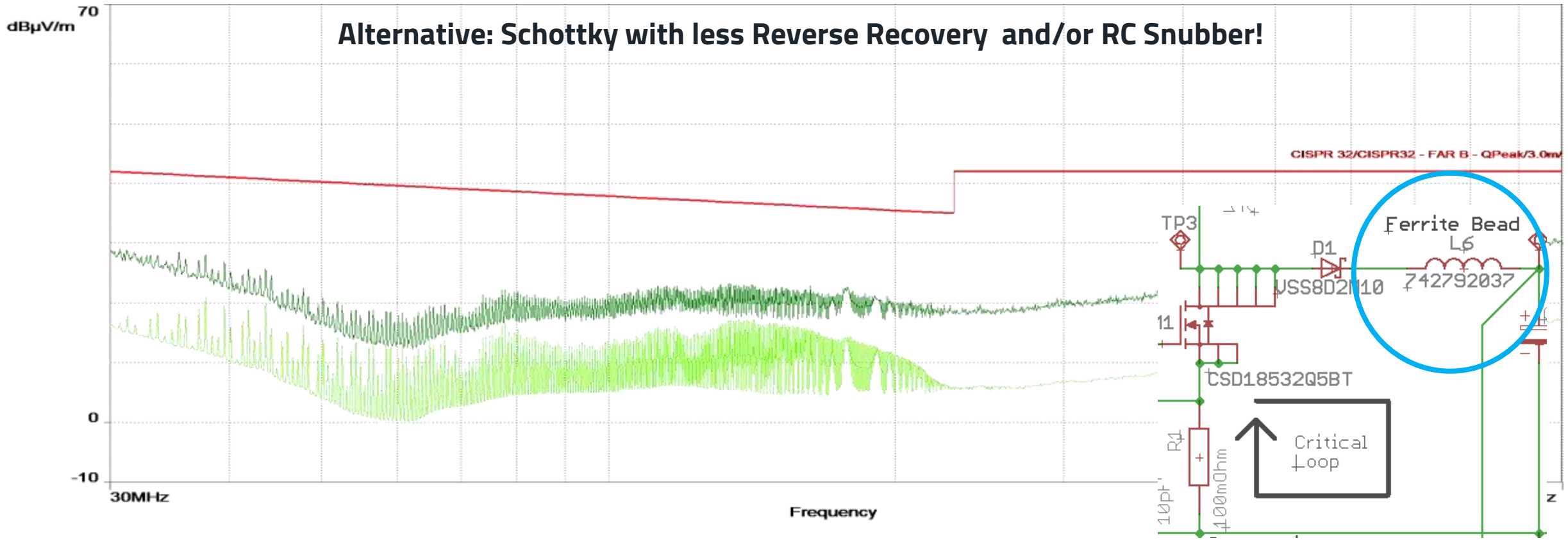


$$L = \frac{X_L}{2 \cdot \pi \cdot f} = \frac{7\Omega}{2\pi 10MHz} = 11nH$$



EMC Test Lab

CISPR32 Radiated Emission



Good Design: No Filters but with Chip Bead Ferrite after Schottky Diode

Redexpert

SL5 CMC Selection

REDEXPERT® | CM CHOKES FOR LOW VOLTAGE AND DATA LINES | APPLICATIONS | HOW TO | SHARE | ITEMS | ANDREAS

Filters: Series = WE-SL5 — 9 items

Order Code	Series	Size	Spec	V_R	Z	L_0	I_R	Winding Style	Length	Width	Height	Lines	T_{max}	Assemb...
744272221	WE-SL5	1087		80.0 V	780 Ω	220 µH	2.20 A	sectional	10.0 mm	8.70 mm	6.30 mm	2	125°C	SMT
744272222	WE-SL5	1087		80.0 V	7.50 kΩ	2.20 mH	750 mA	bifilar	10.0 mm	8.70 mm	6.30 mm	2	125°C	SMT
744272251	WE-SL5	1087		80.0 V	970 Ω	250 µH	2.00 A	sectional	10.0 mm	8.70 mm	6.30 mm	2	125°C	SMT
744272332	WE-SL5	1087		80.0 V	8.90 kΩ	3.30 mH	650 mA	bifilar	10.0 mm	8.70 mm	6.30 mm	2	125°C	SMT
744272392	WE-SL5	1087		80.0 V	9.60 kΩ	3.90 mH	520 mA	bifilar	10.0 mm	8.70 mm	6.30 mm	2	125°C	SMT
744272471	**WE-SL5**	**1087**		**80.0 V**	**1.75 kΩ**	**470 µH**	**1.60 A**	**sectional**	**10.0 mm**	**8.70 mm**	**6.30 mm**	**2**	**125°C**	**SMT**
744272472	WE-SL5	1087		80.0 V	13.0 kΩ	4.70 mH	350 mA	bifilar	10.0 mm	8.70 mm	6.30 mm	2	125°C	SMT

744272471 — WE-SL5 · 1087 — 1.75 kΩ · 1.60 A · sectional

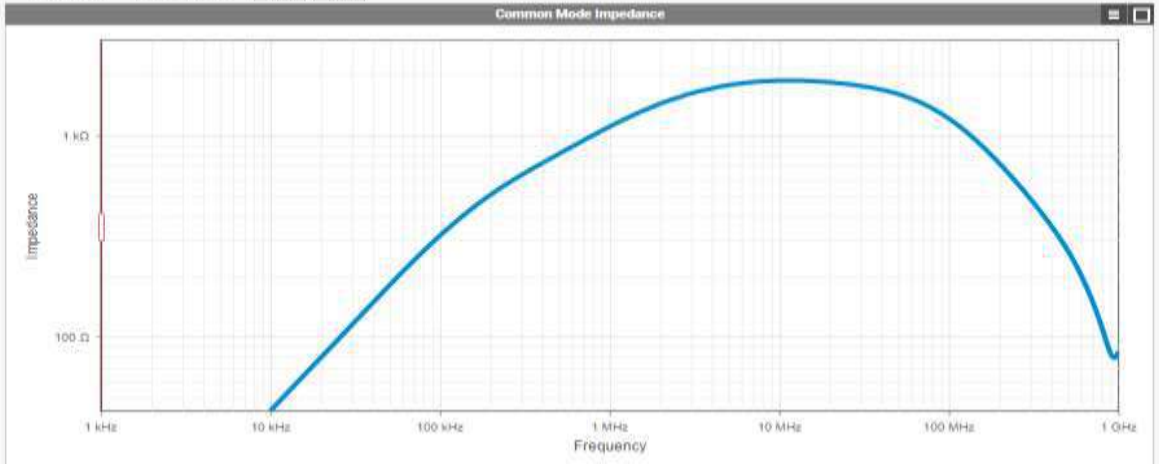
Click and type or drop an Order Code here

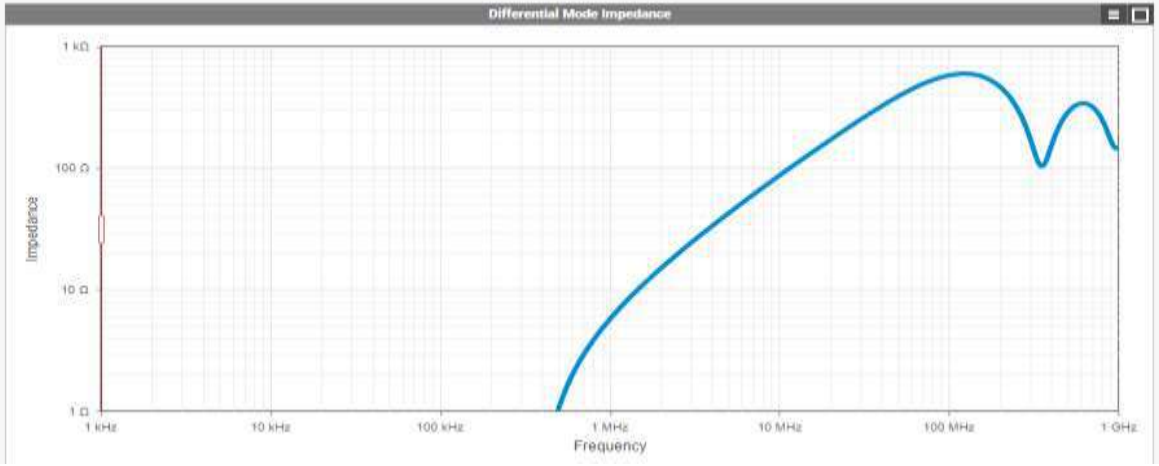
ADD

MORE

Z = Over 1kΩ from 1MHz to 150MHz

Show Panel: CMA DMA CMI DMI





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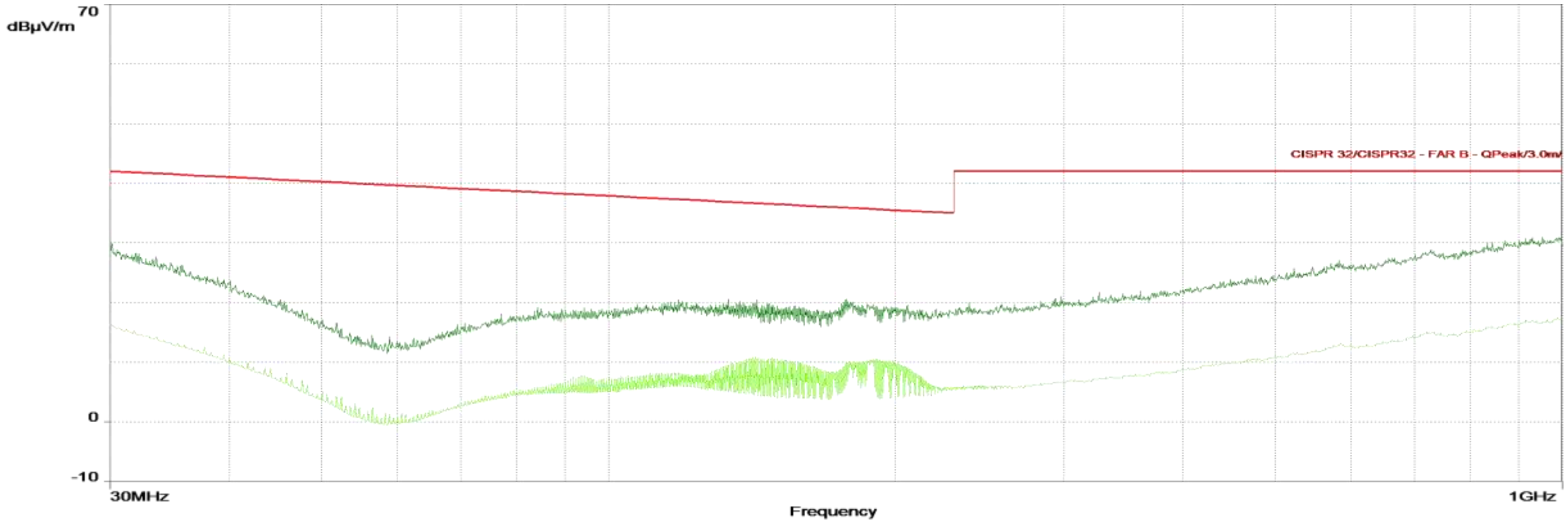
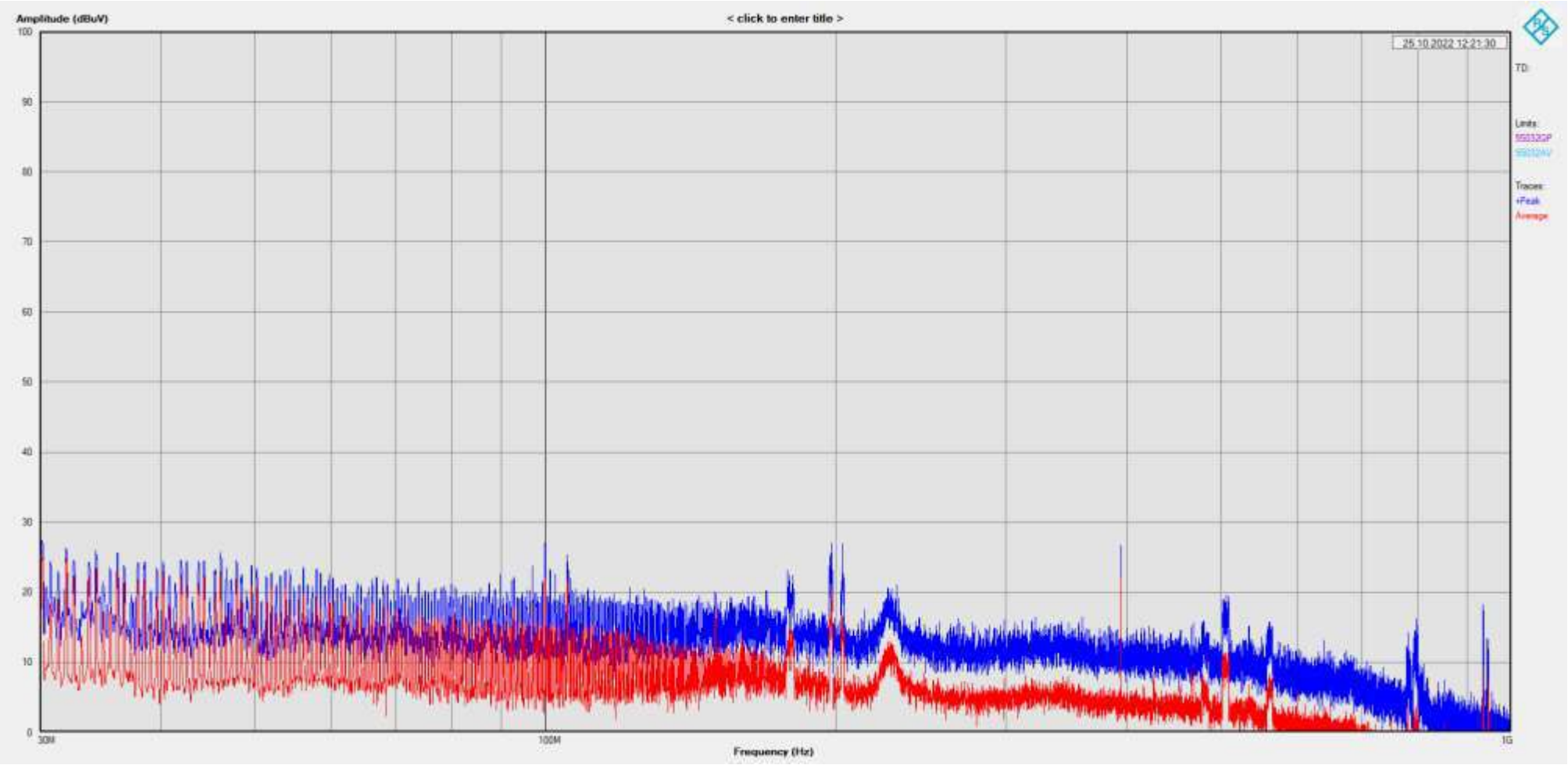


Good Design: With all Filters and Chip Bead Ferrite after Schottky Diode

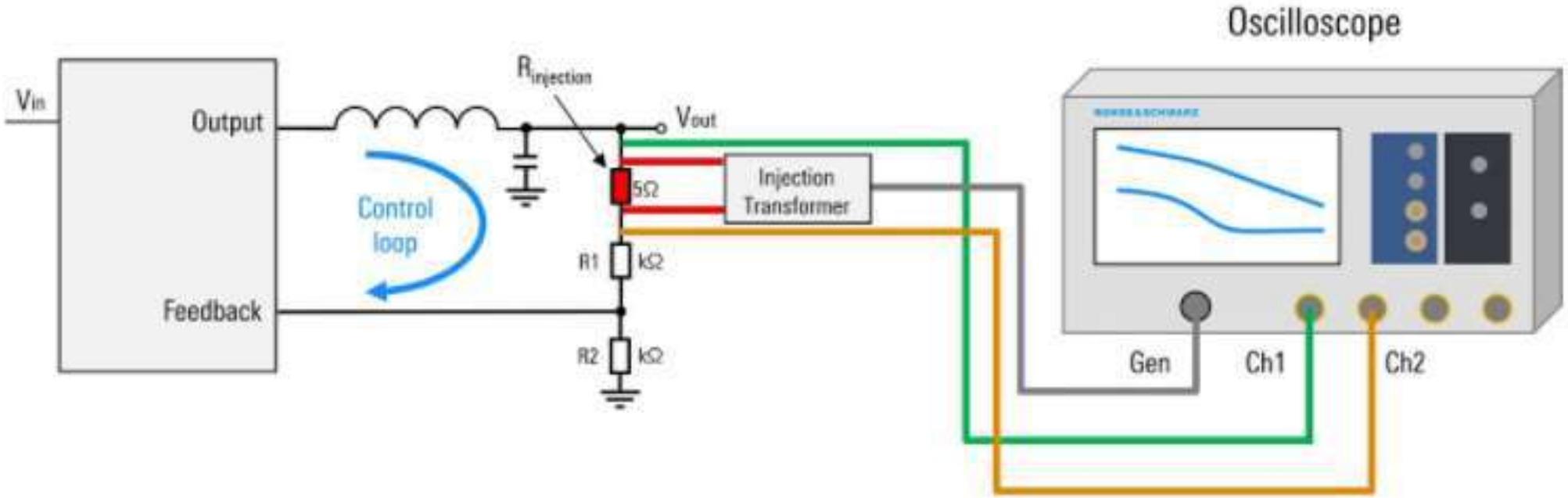
EMC Measurement 1GHz

FAE Equipment Good Design CM



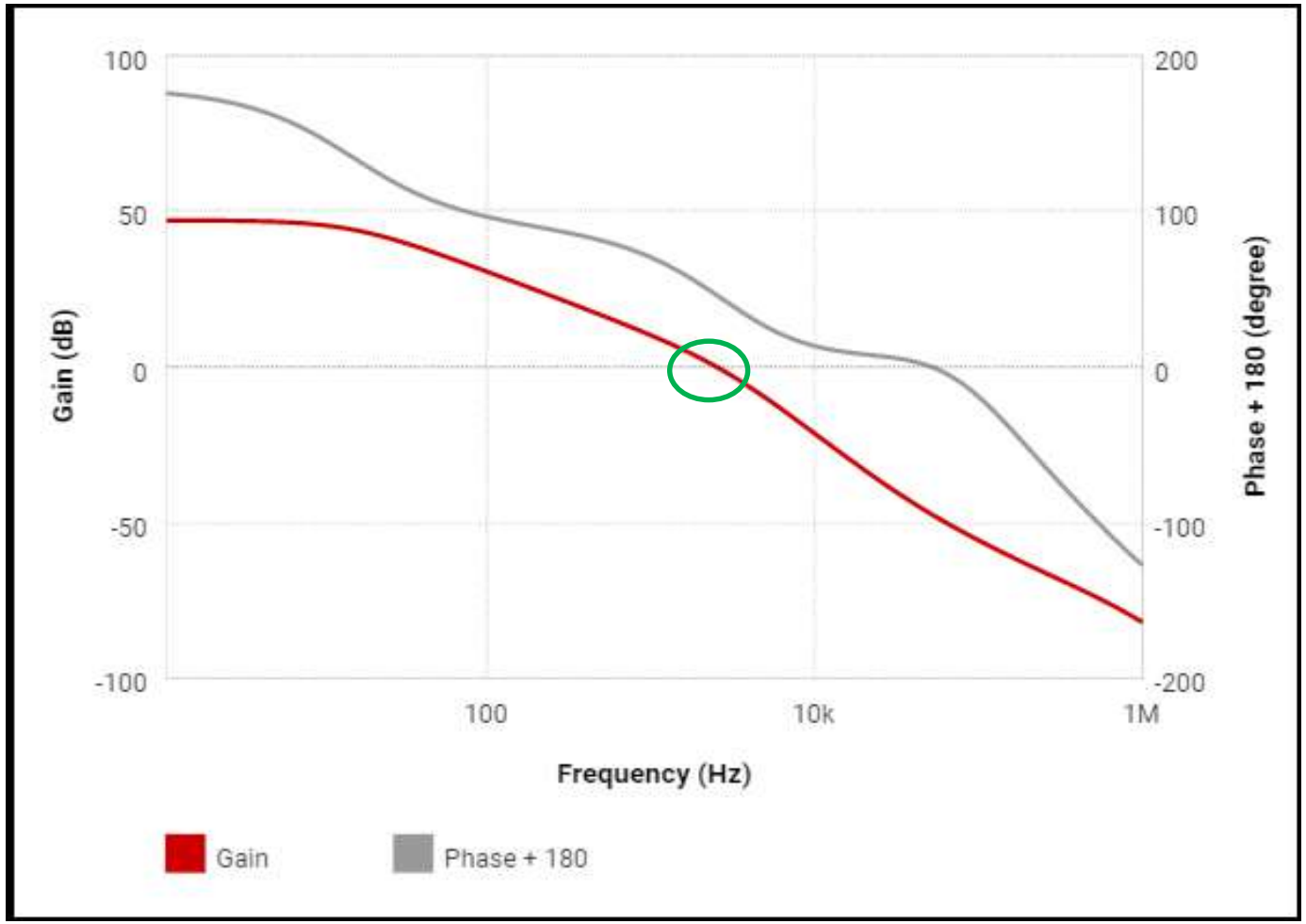
Regulation Loop RTA4004 Measurement

Measurement Setup



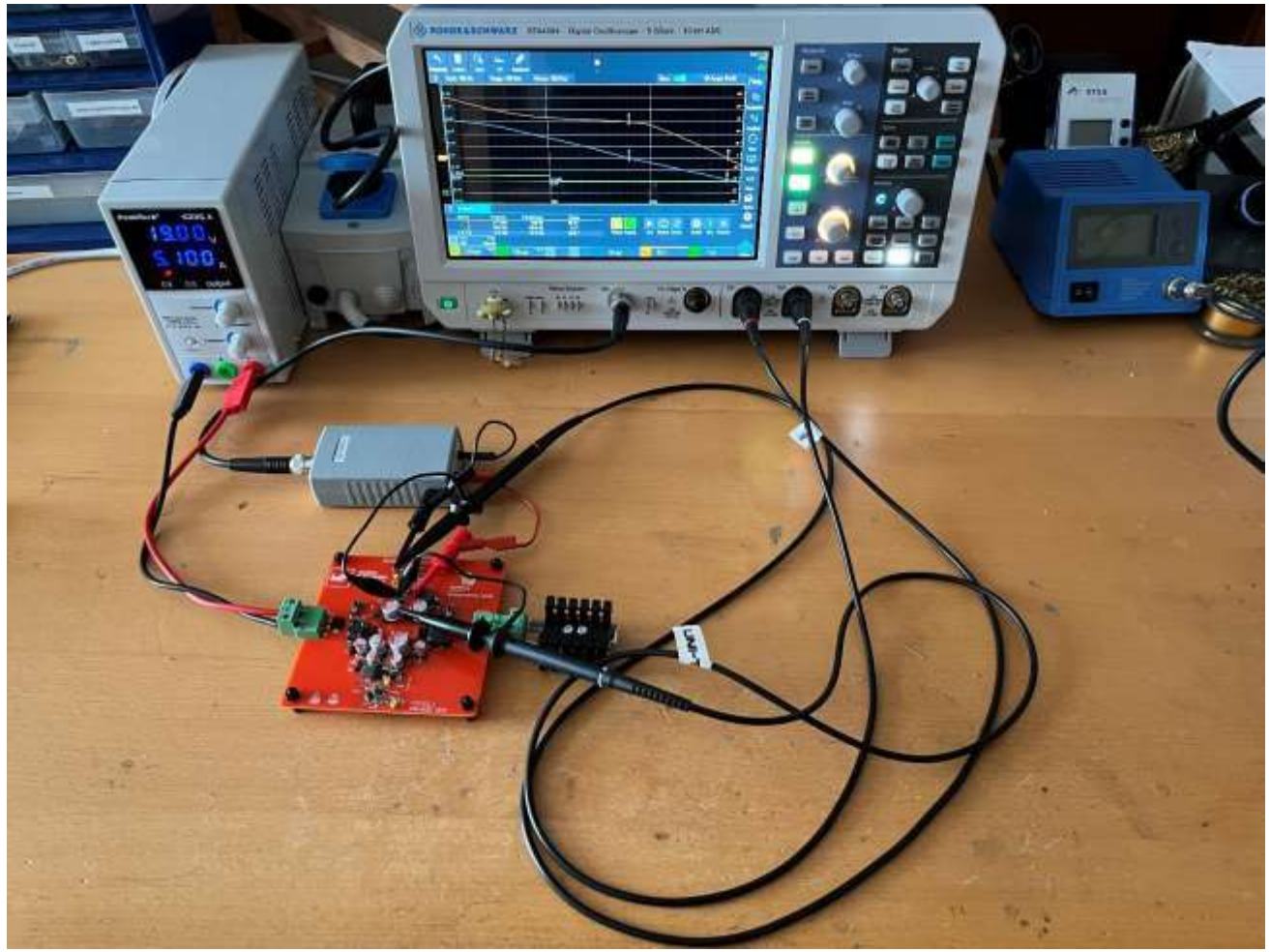
Regulation Loop Bode Plot Simulation

0dB crossing at around 6kHz(Simulation TI Webbench)



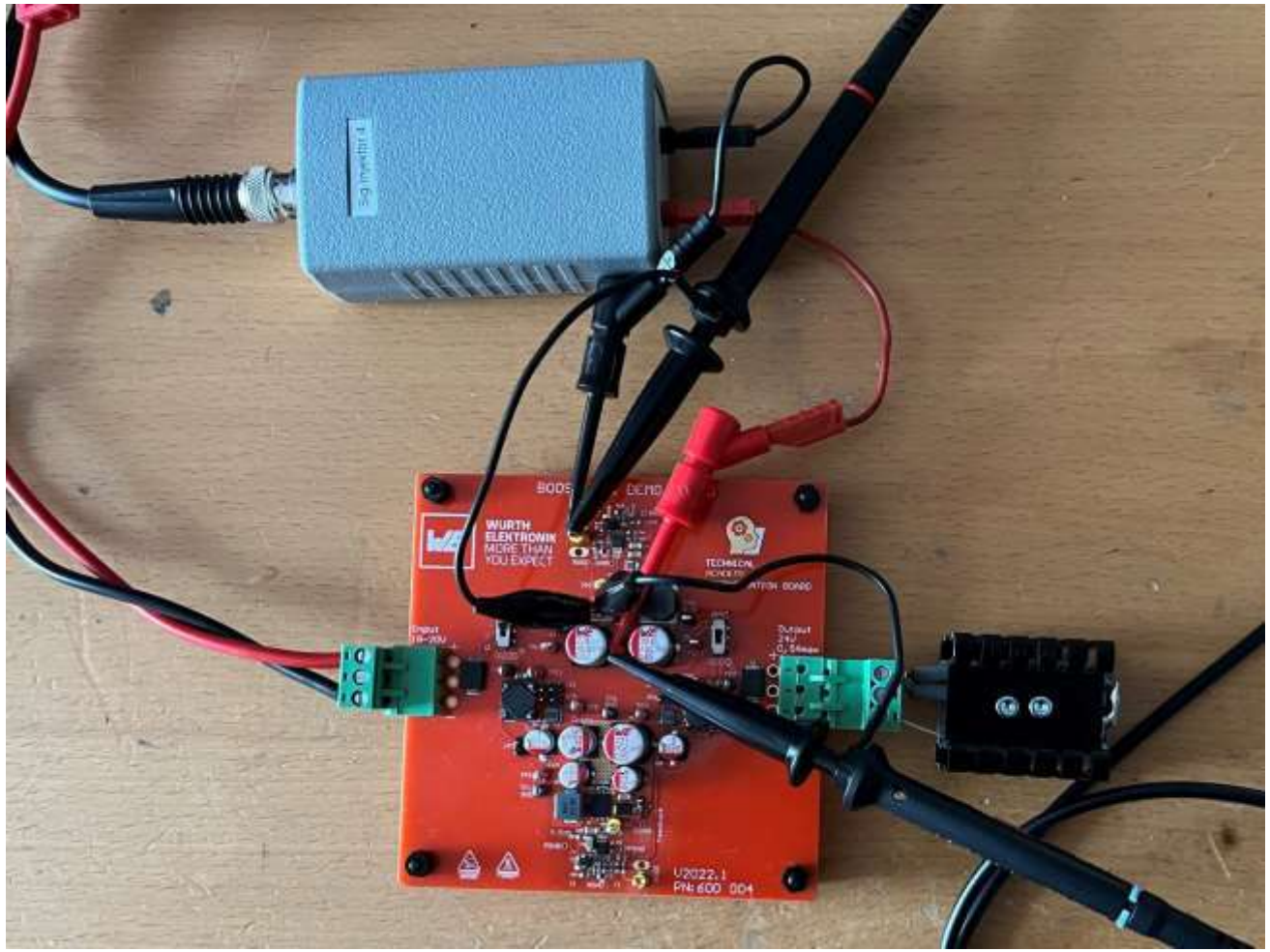
Regulation Loop - RTA4004 Measurement

Measurement Setup

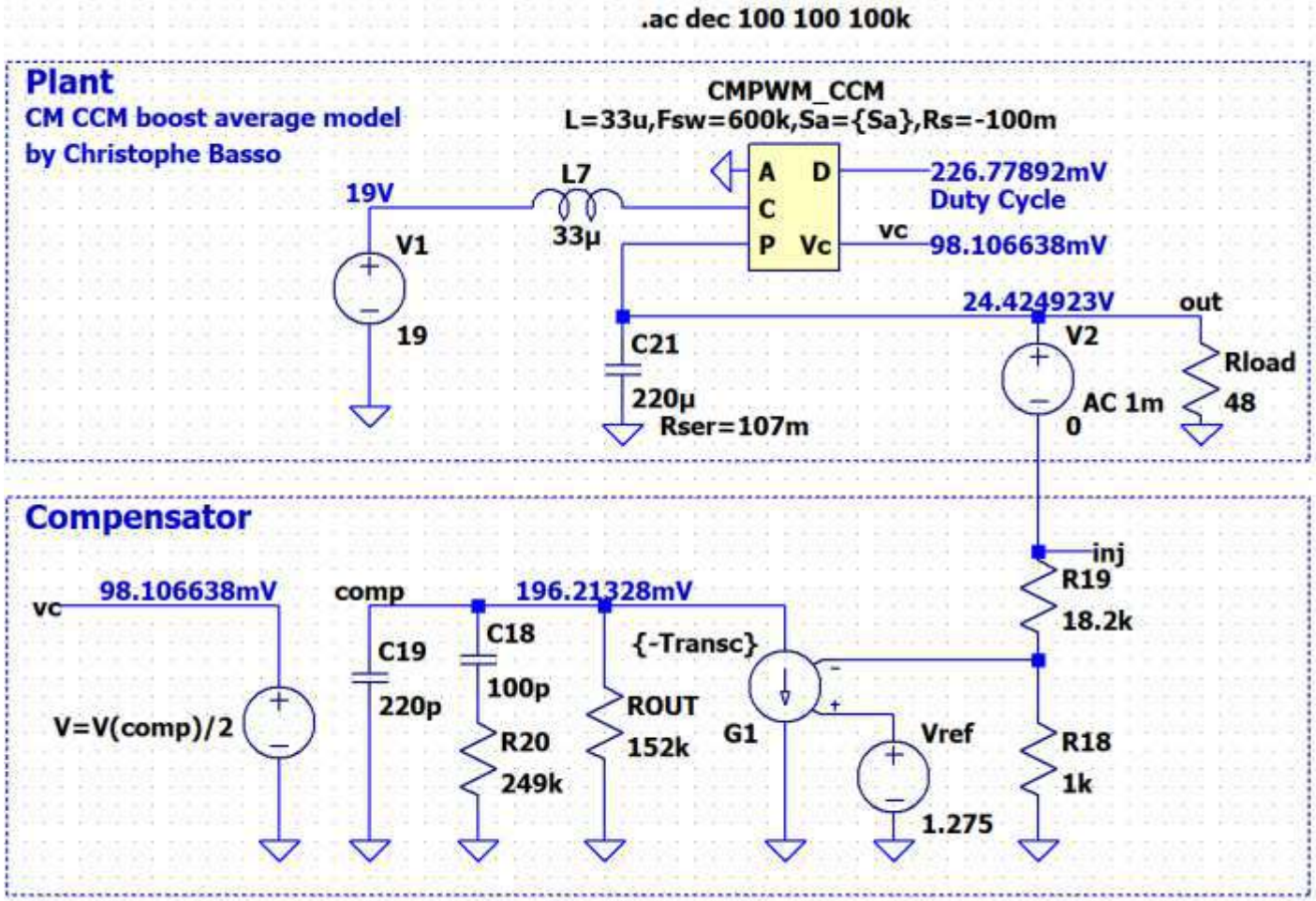


Loop Bad Design - RTA4004 Measurement

Measurement Setup



Loop Bad Design - LTSpice - Average model



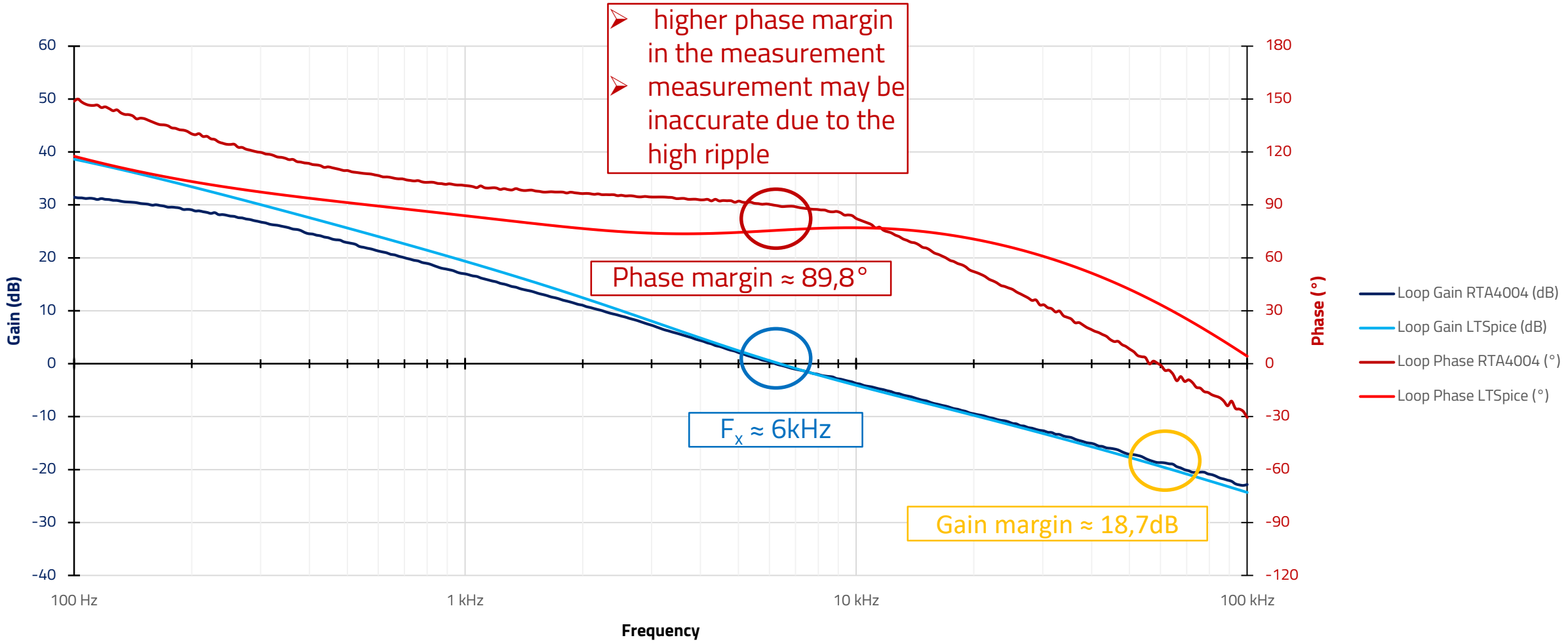
from IC-datasheet LM3481:

Slope Compensation:

Sa = (VSL + dVSL) x Fsw
= (VSL + k x RSL) x Fsw
= (90mV + 40µA x 100Ohm) x 600kHz =56.4kV/s

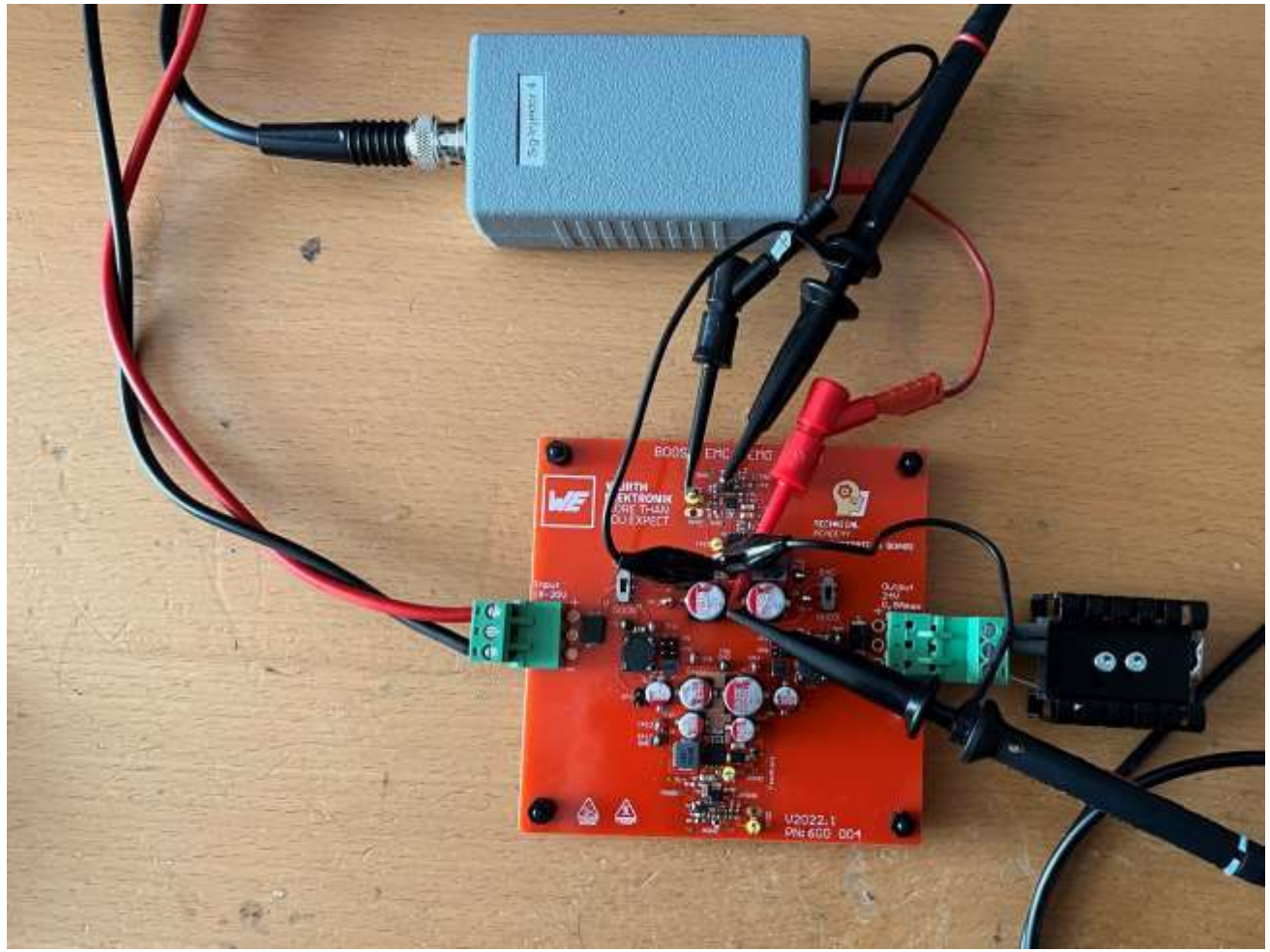
.param Sa=56.4k
.param Transc=450u

Loop Bad Design - RTA4004 Measurement vs. LTSpice Simulation



Plant Bad Design - RTA4004 Measurement

Measurement Setup



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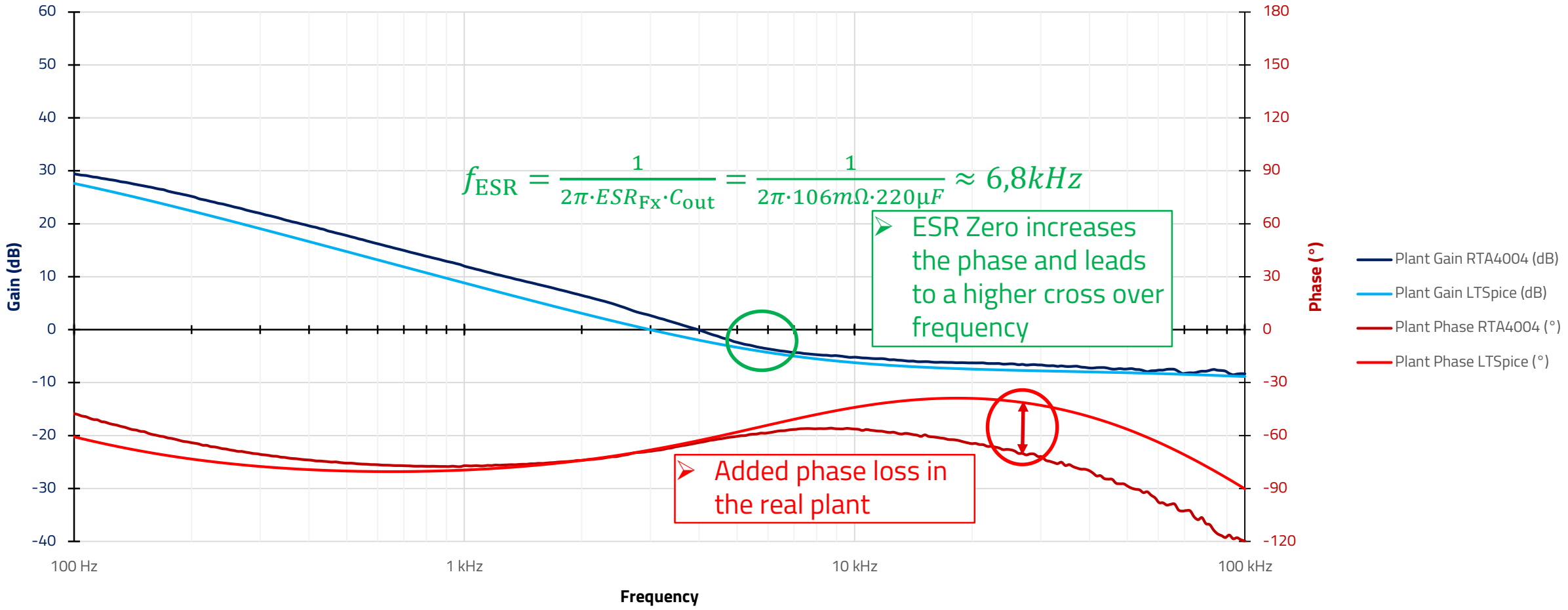
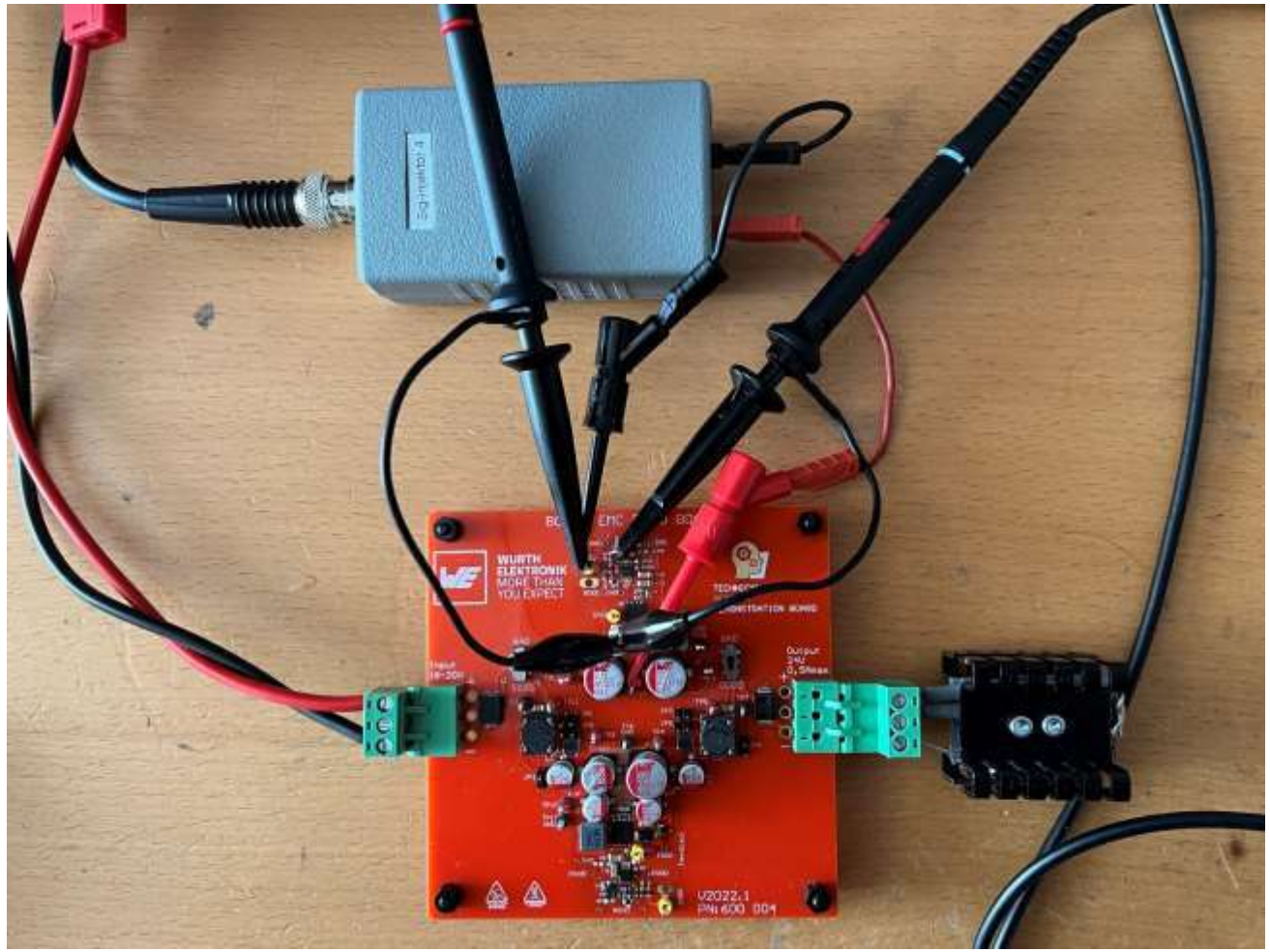
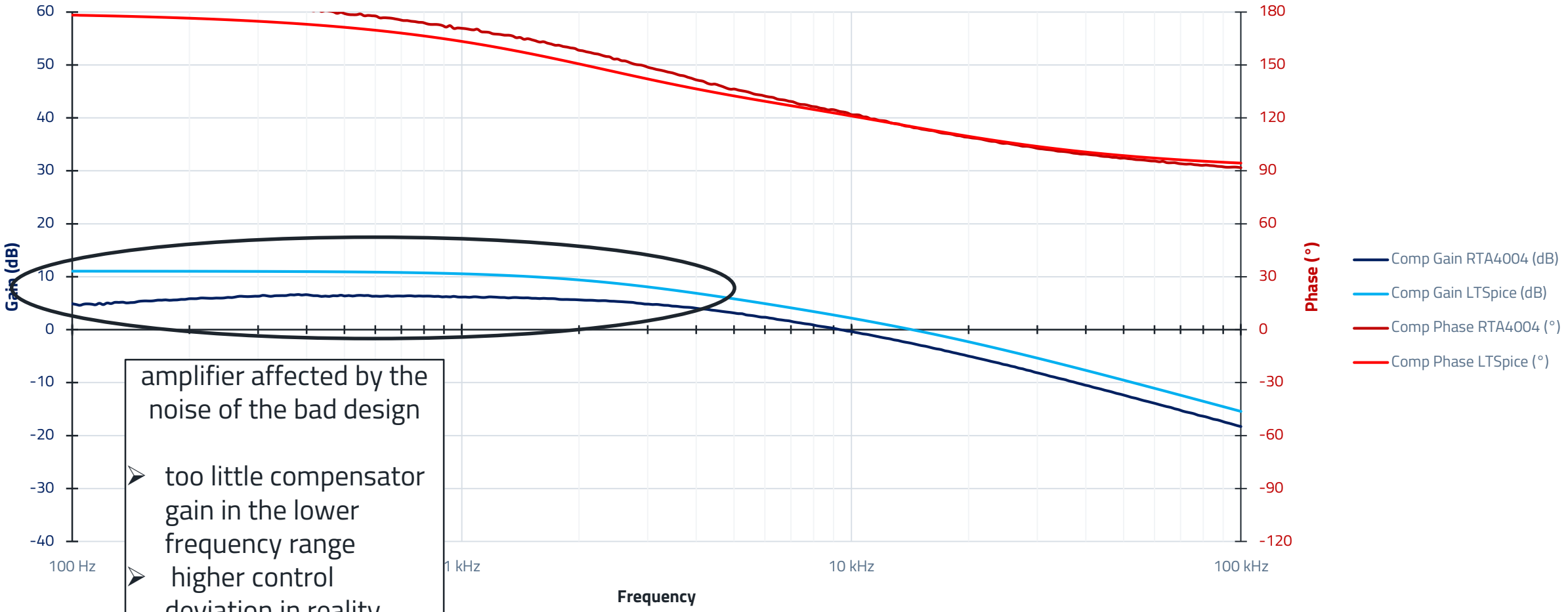


Compensator Bad Design - RTA4004 Measurement

Measurement Setup



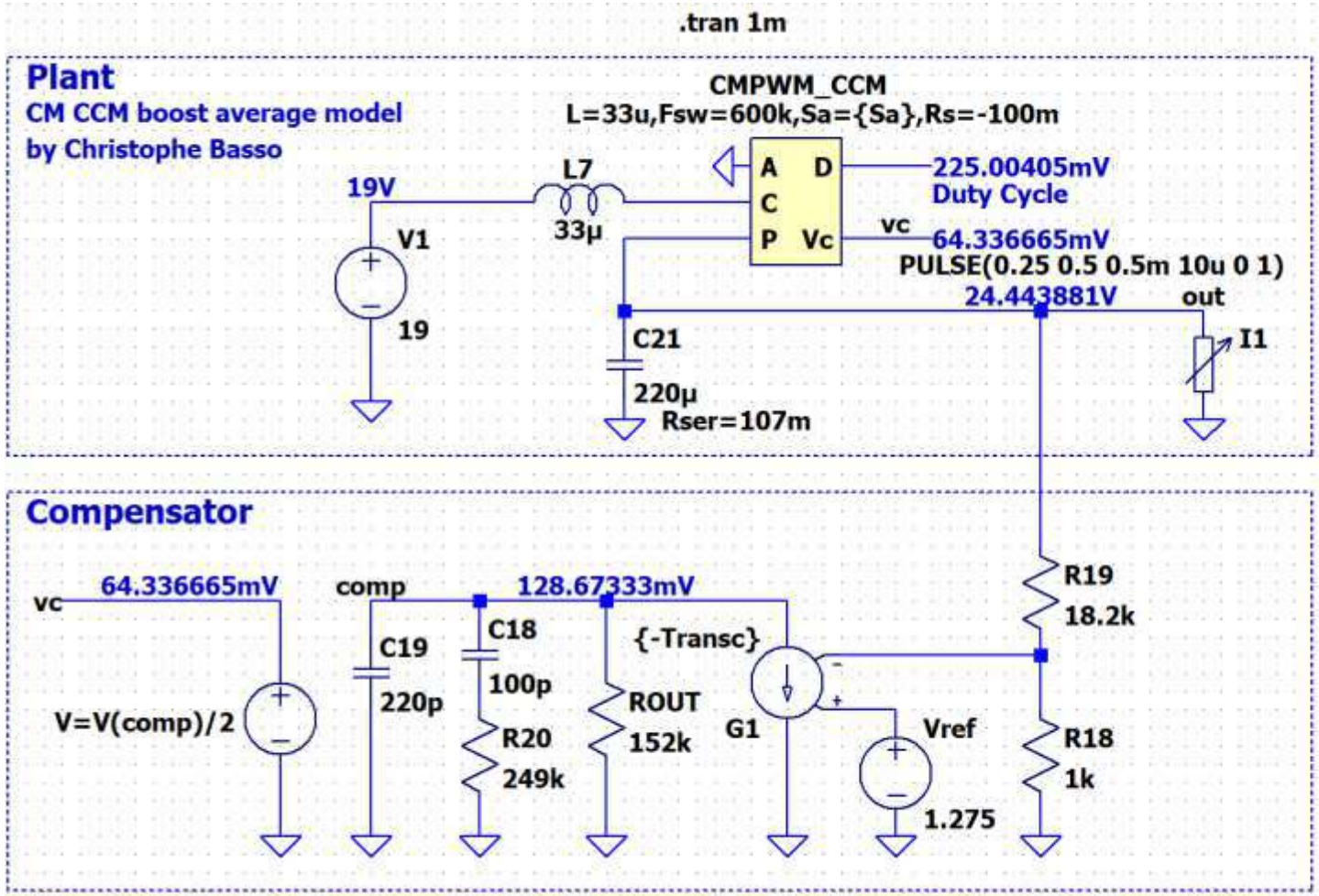
Compensator Bad Design - RTA4004 Measurement vs. LTSpice Simulation



amplifier affected by the noise of the bad design

- too little compensator gain in the lower frequency range
- higher control deviation in reality

Load Step Bad Design - LTSpice - Average model



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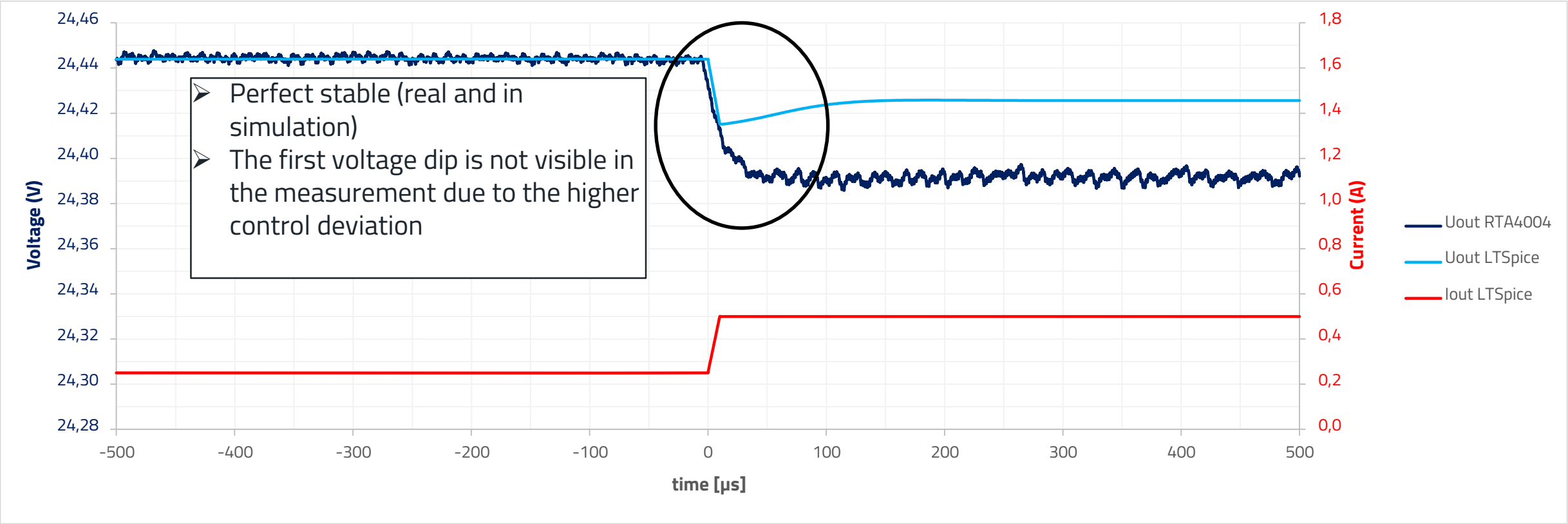
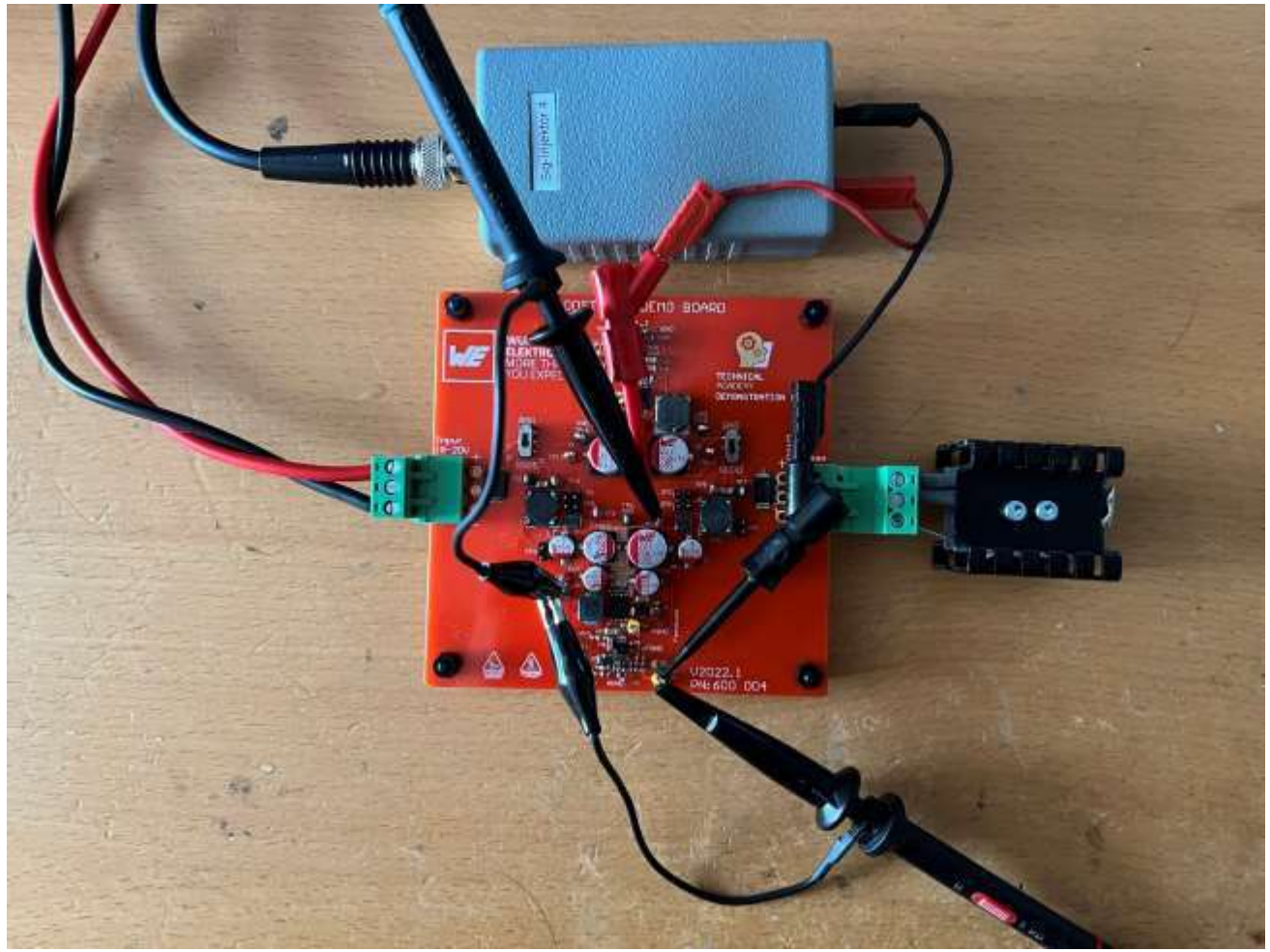
Load step Bad Design - RTA4004 Measurement vs. LTSpice Simulation



Loop Good Design RTA4004 Measurement

Measurement Setup



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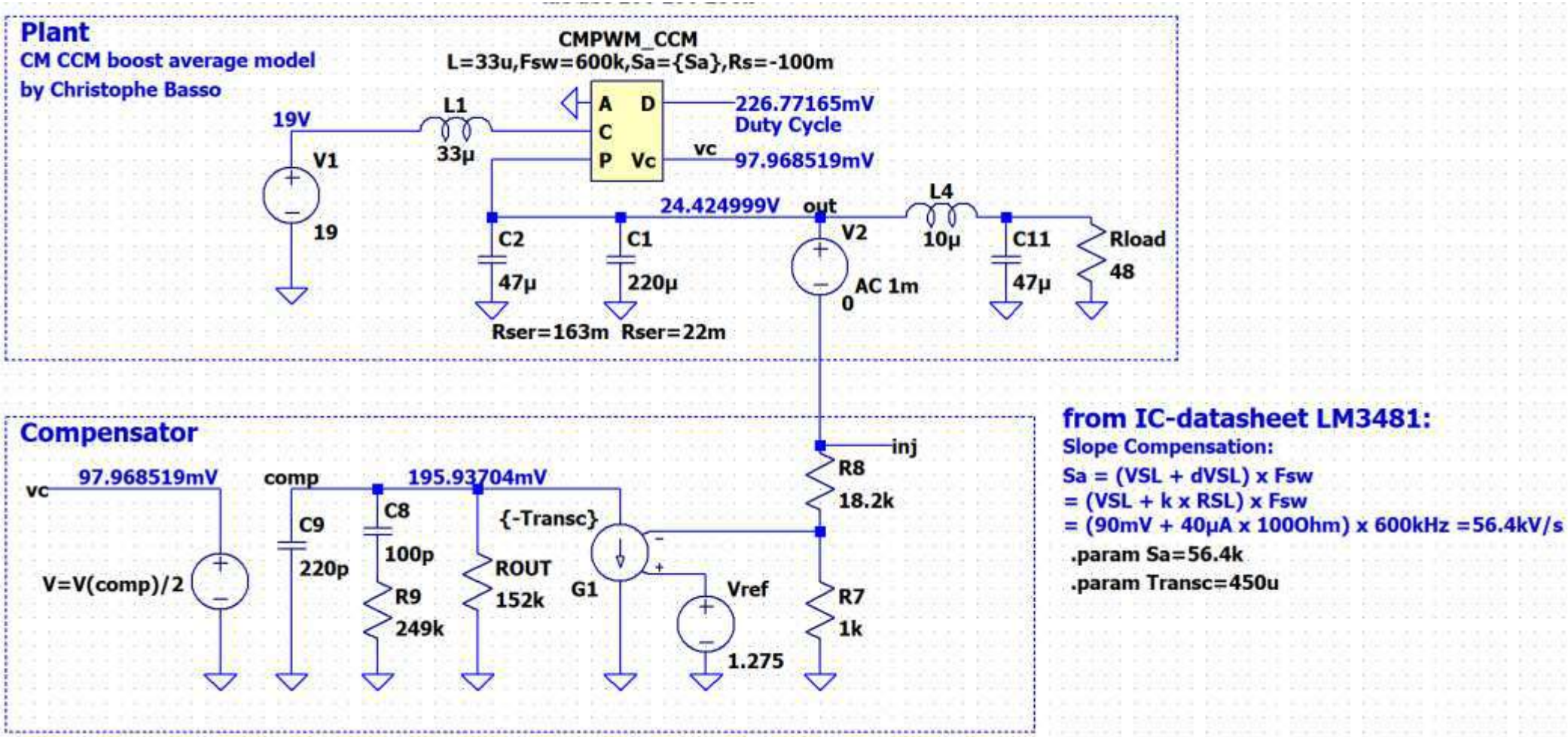

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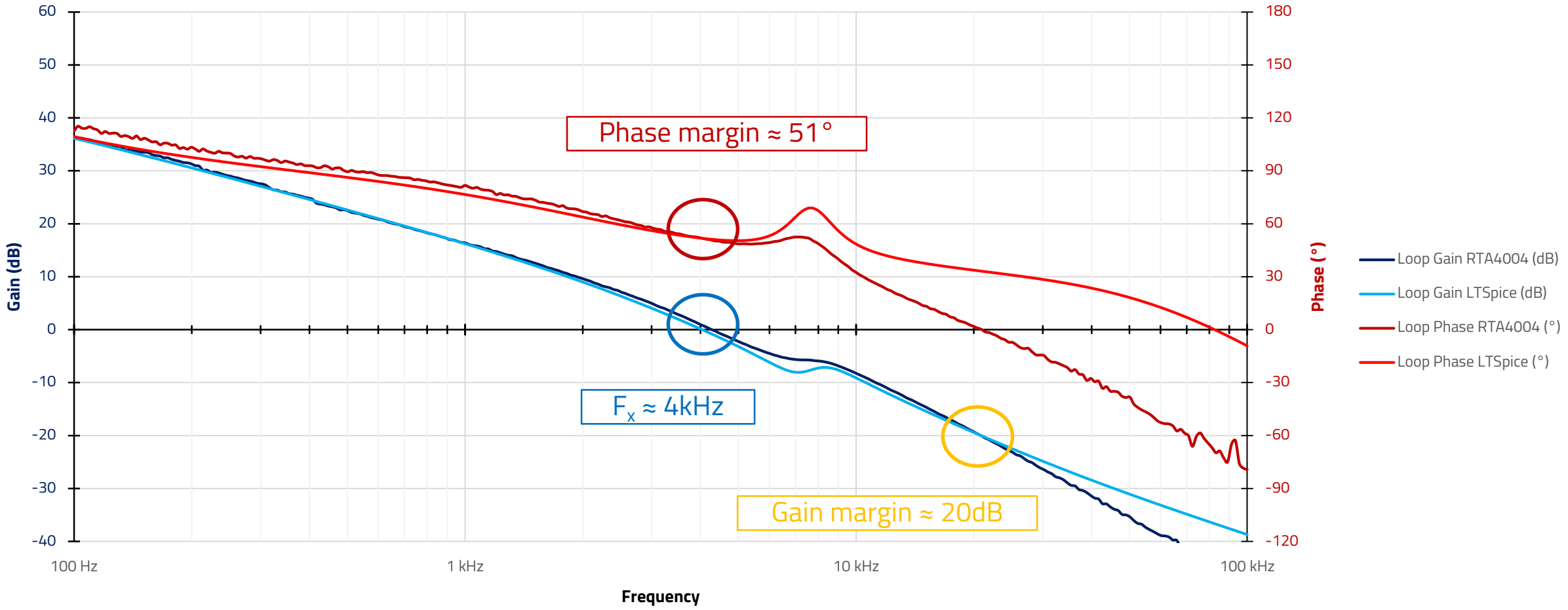
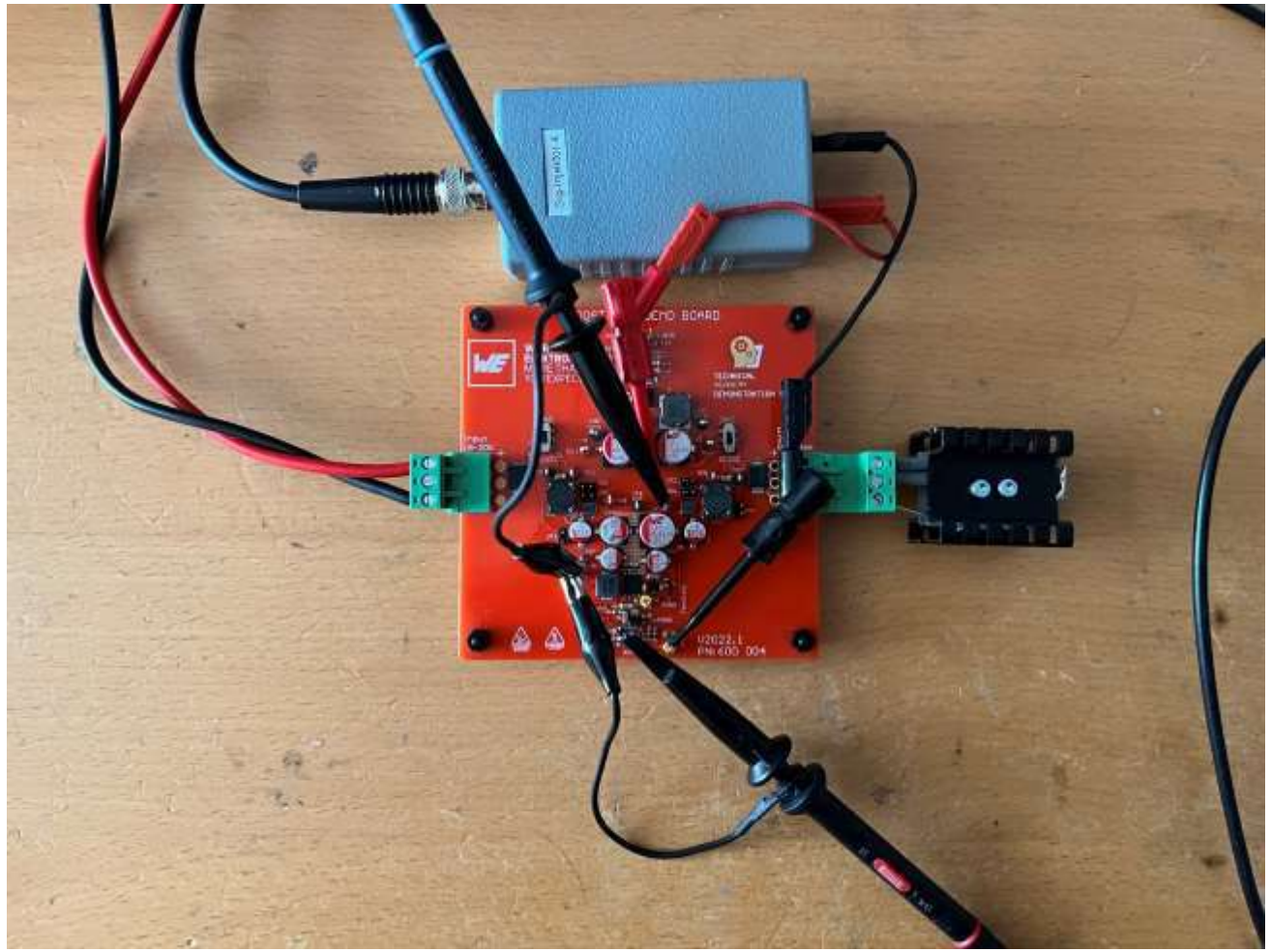


Plant Good Design - RTA4004 Measurement

Measurement Setup



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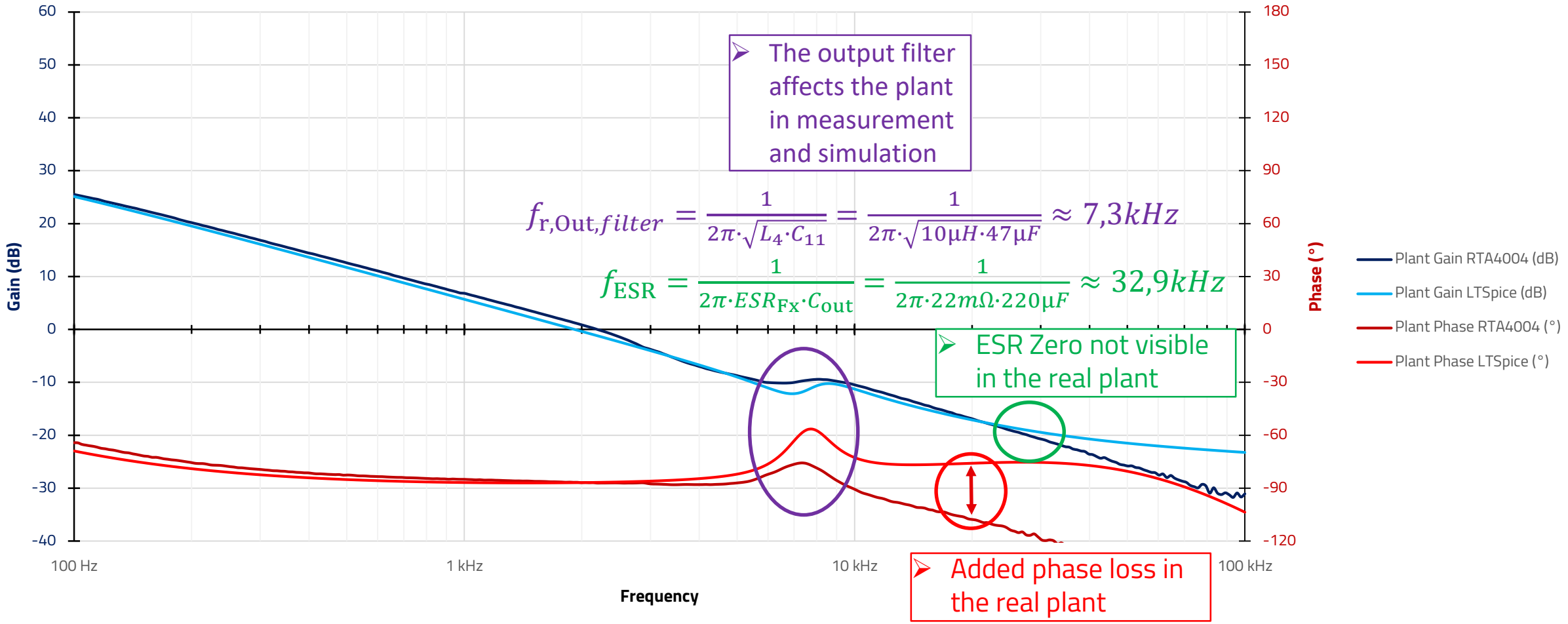

Compensator Good Design - RTA4004 Measurement

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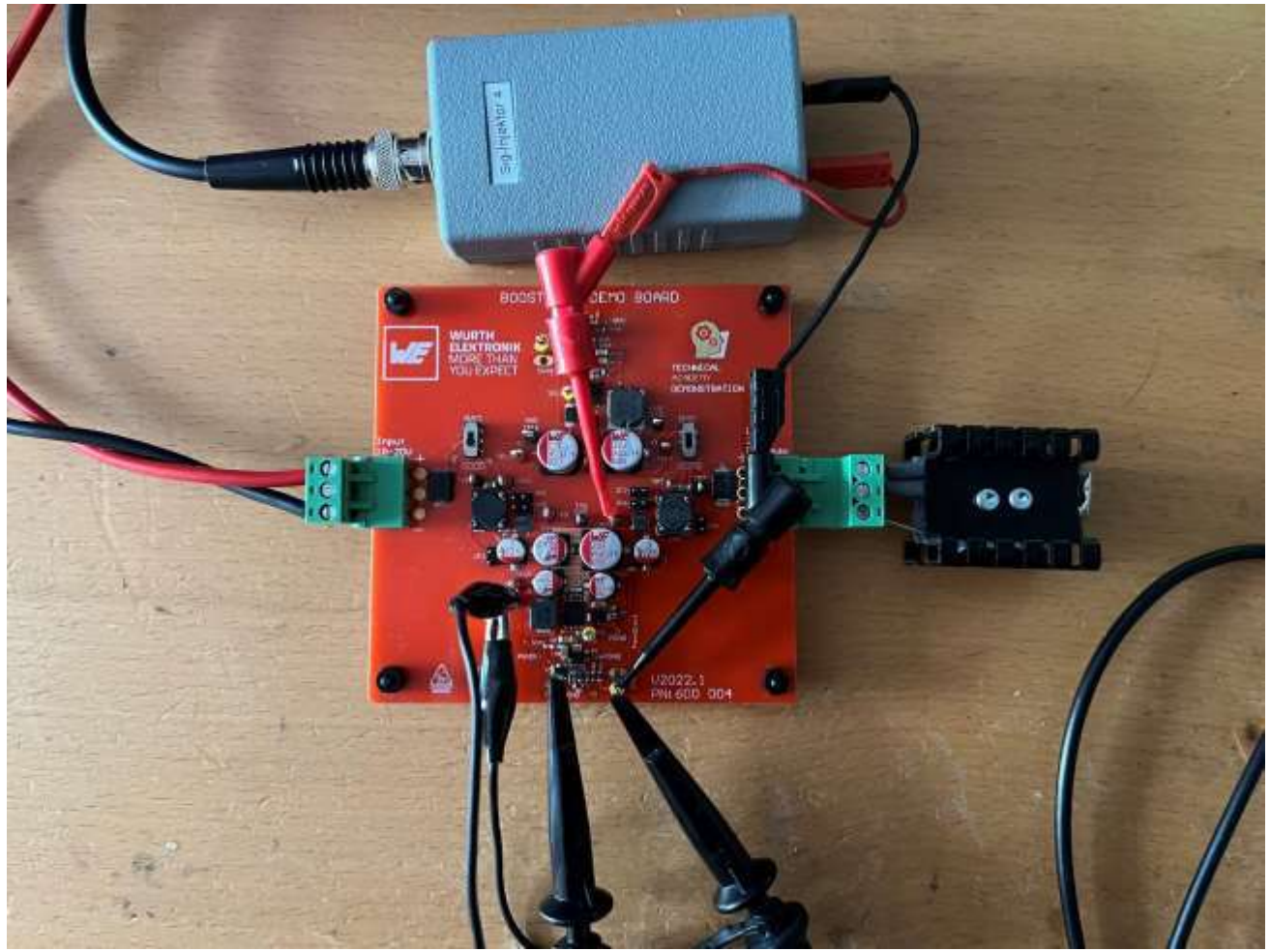

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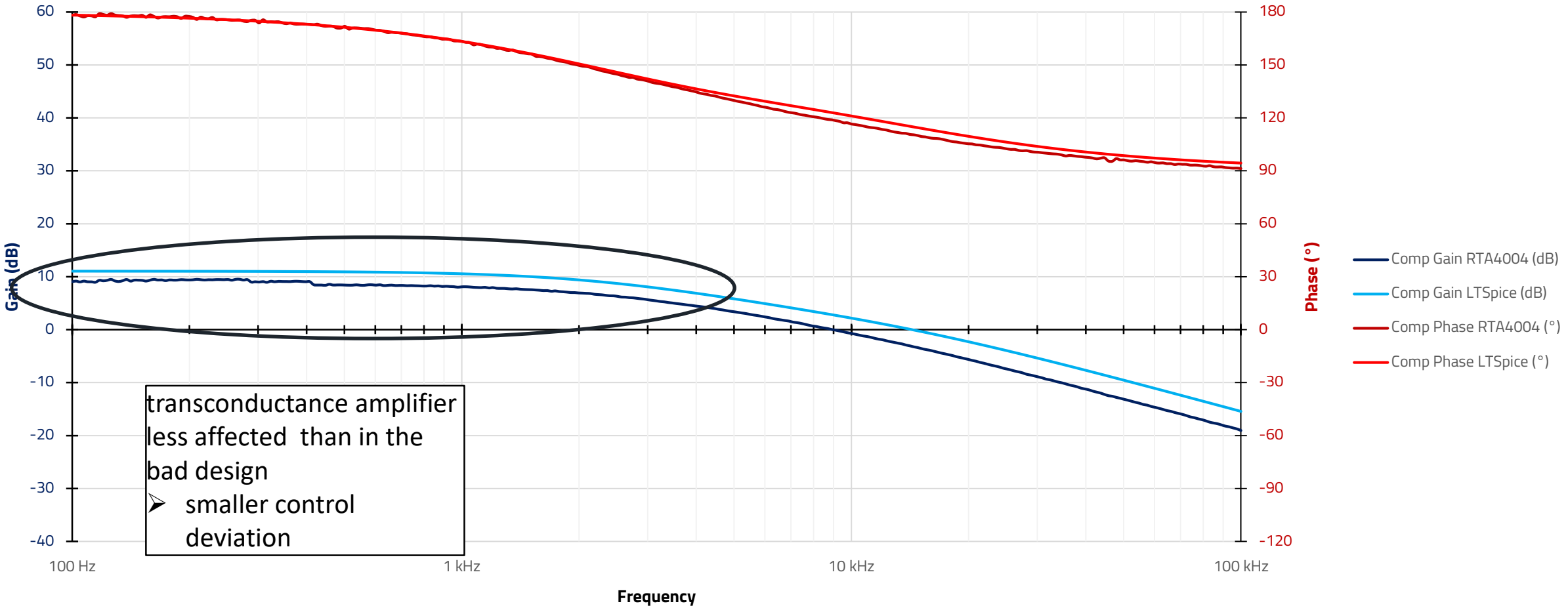
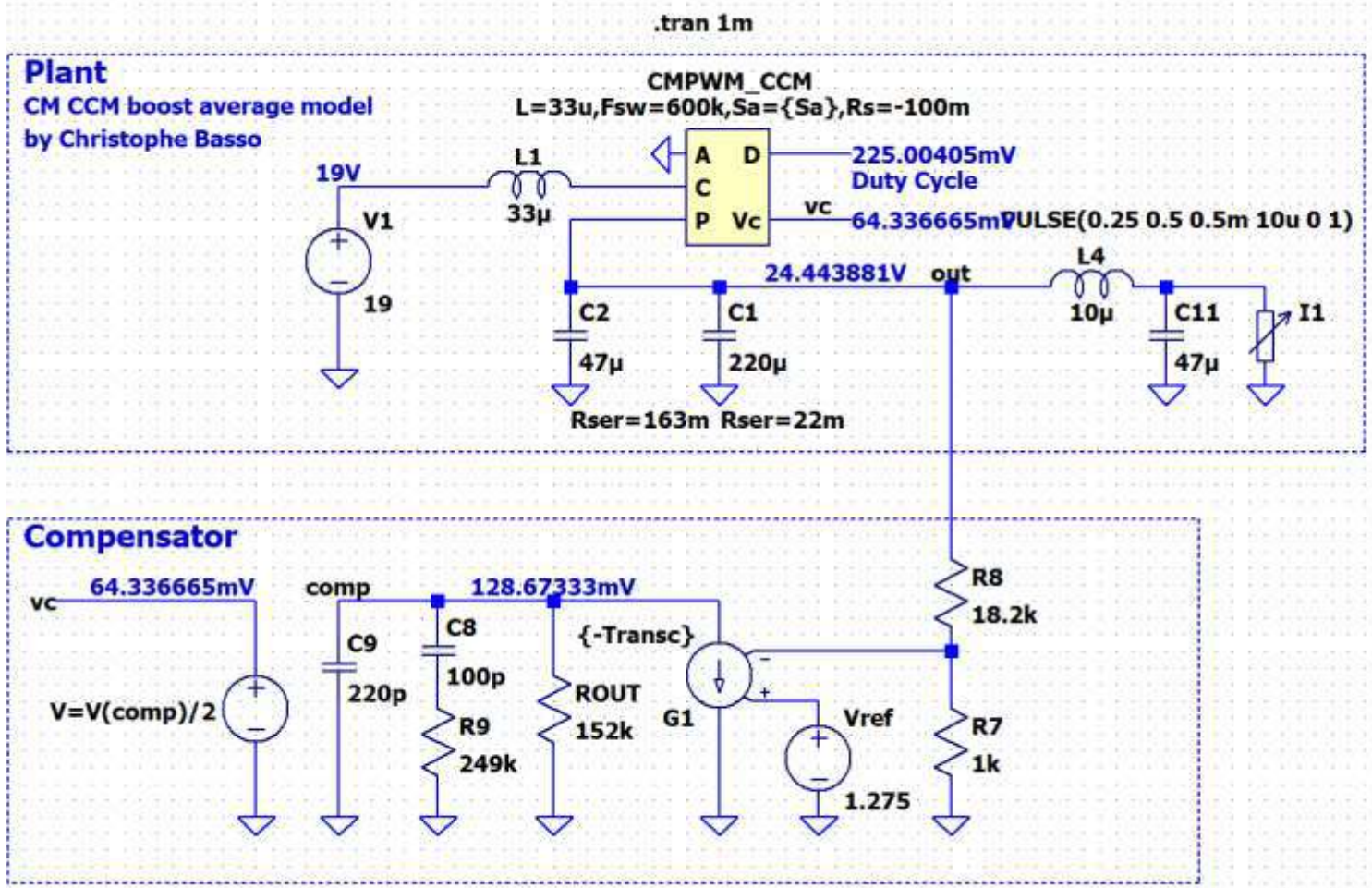


transconductance amplifier less affected than in the bad design

- smaller control deviation

Load step Good Design - RTA4004 Measurement vs. LTSpice Simulation



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